phyCARD-S

Hardware Manual

Document No.:	L-731e_1
SBC Prod. No.:	PCA-A-S1-xxx
CB Prod. No.:	PBA-A-01
Edition:	April 2010

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1st Edition April 2010

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Conventions, Abbreviations and Acronyms

This hardware manual describes the PCA-A-S1 Single Board Computer in the following referred to as phyCARD-S. The manual specifies the phyCARD-S's design and function. Precise specifications for the Freescale i.MX27 microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by a "n", "/", or “#”character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{\text{RD}}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- Tables which describe jumper settings show the default position in **bold, blue text**.
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the *phyCARD-Connector* always refer to the high density molex connector on the undersides of the phyCARD-S Single Board Computer.

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows, or Linux) preinstalled on the module and Development Tools).
GPIO	General purpose input and output.

GPI	General purpose input.
GPO	General purpose output.
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the Carrier Board.
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the Carrier Board.
CB	Carrier Board; used in reference to the phyBASE Development Kit Carrier Board.
DFF	D flip-flop.
EMB	External memory bus.
EMI	Electromagnetic Interference.
IRAM	Internal RAM; the internal static RAM on the Freescale i.MX27 microcontroller.
J	Solder jumper; these types of jumpers require solder equipment to remove and place.
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools.
PCB	Printed circuit board.
RTC	Real-time clock.
SMT	Surface mount technology.
SBC	Single Board Computer; used in reference to the PCA-A-S1 /phyCARD-A-S1 Single Board Computer
VBAT	SBC standby voltage input

Table 1: Abbreviations and Acronyms used in this Manual

Note: The BSP delivered with the phyCARD-S usually includes drivers and/or software for controlling all components such as interfaces, memory, etc.. Therefore programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the i.MX27 Reference Manual, if such information is needed to connect customer designed applications.

Preface

As a member of PHYTEC's new phyCARD product family the phyCARD-S is one of a series of PHYTEC Single Board Computers (SBCs) that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCARD OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SBC subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyCARD module lies in its layout and test.

PHYTEC's new phyCARD product family consists of a series of extremely compact embedded control engines featuring various processing performance classes while using the newly developed X-Arc embedded bus standard. The standardized connector footprint and pin assignment of the X-Arc bus makes this new SBC generation extremely scalable and flexible. This also allows to use the same carrier board to create different applications depending on the required processing power. With this new SBC concept it is possible to design entire embedded product families around vastly different processor performances while optimizing overall system cost. In addition, future advances in processor technology are already considered with this new embedded bus standard making product upgrades very easy. Another major advantage is the forgone risk of potential system hardware redesign steps caused by processor or other critical component discontinuation. Just use one of PHYTEC's other phyCARD SBCs

thereby ensuring an extended product life cycle of your embedded application.
Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce your development time and risk and allow you to focus on your product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution you will be able to bring your new ideas to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.com/services/

Ordering Information

The part numbering of the phyCARD has the following structure:

PCA-A-S1-*xxxxxx*

Generation

A = First generation

Performance class

S = small
M = middle
L = large
XL = largest

Controller Number of specified performance class

Assembly options (depending on model)

In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at

http://www.phytec.de/de/support/registrierung.html

You can also get technical support and additional information concerning your product.

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The support section of our web site provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/de/support/faq/faq-phycard-s.html

Declaration of Electro Magnetic Conformity of the PHYTEC phyCARD-S

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

1 Introduction

The phyCARD-S belongs to PHYTEC’s phyCARD Single Board Computer module family. The phyCARD SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCARD boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

PHYTEC's phyCARD family introduces the newly developed X-Arc embedded bus standard. Apart from processor performance, a large number of embedded solutions require a corresponding number of standard interfaces. Among these process interfaces are for example Ethernet, USB, UART, SPI, I^2C, audio, display and camera connectivity. The X-Arc bus exactly meets this requirement. As well the location of the commonly used interfaces as the mechanical specifications are clearly defined. All interface signals of PHYTEC's new X-Arc bus are available on a single, 100-pin , high-density pitch (0.635 mm) connector, allowing the phyCARDs to be plugged like a "big chip" into a target application. The reduced complexity of the phyCARD SBC as well as the smaller number of interface signals greatly simplifies the SBC carrier board design helping you to reduce your time-to-market.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments approximately 20 % of all pin header connectors on the X-Arc bus are dedicated to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCARD boards even in high noise environments.

phyCARD boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyCARD users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCARD-S is a subminiature (60 x 60 mm) insert-ready Single Board Computer populated with the Freescale i.MX27 microcontroller. Its universal design enables its insertion in a wide range of embedded applications.

Precise specifications for the controller populating the board can be found in the applicable controller Reference Manual or datasheet. The descriptions in this manual are based on the Freescale i.MX27. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCARD-S.

The phyCARD-S offers the following features:

- Subminiature Single Board Computer (´60 x 60 mm) achieved through modern SMD technology
- Populated with the Freescale i.MX27 microcontroller (BGA404 packaging)
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- X-Arc bus including commonly used interfaces such as Ethernet, USB, UART, SPI, I^2C, audio, display and camera connectivity (both LVDS) available at one 100-pin high-density (0.635 mm) Molex connector, enabling the phyCARD-S to be plugged like a "big chip" into target application
- Max. 400 MHz core clock frequency
- Boot from NAND Flash
- 128 MByte (up to 1 GByte) on-board NAND Flash[1]
- 32 MByte (up to 512 MByte) Mobile DDR SDRAM on-board
- 4KB (up to 32kB) I^2C EEPROM

[1] Please contact PHYTEC for more information about additional module configurations.

- Serial interface with 4 lines (TTL) allowing simple hardware handshake
- High-Speed USB OTG transceiver
- High-Speed USB HOST transceiver
- Auto HDX/FDX 10/100MBit Ethernet interface, with HP Auto MDI/MDI-X support
- All controller required supplies generated on board
- 4 Channel LVDS (18Bit) LCD-Interface
- Support of standard 20 pin debug interface through JTAG connector
- One I^2C interfaces
- One SPI interfaces
- SD/MMC card interface with DMA
- SSI Interface (AC97)
- Optional LVDS Camera Interface[1]
- 3 GPIO/IRQ ports
- 2 Power State outputs to support applications requiring a power management
- 1 Wake Up input

1.1 Block Diagram

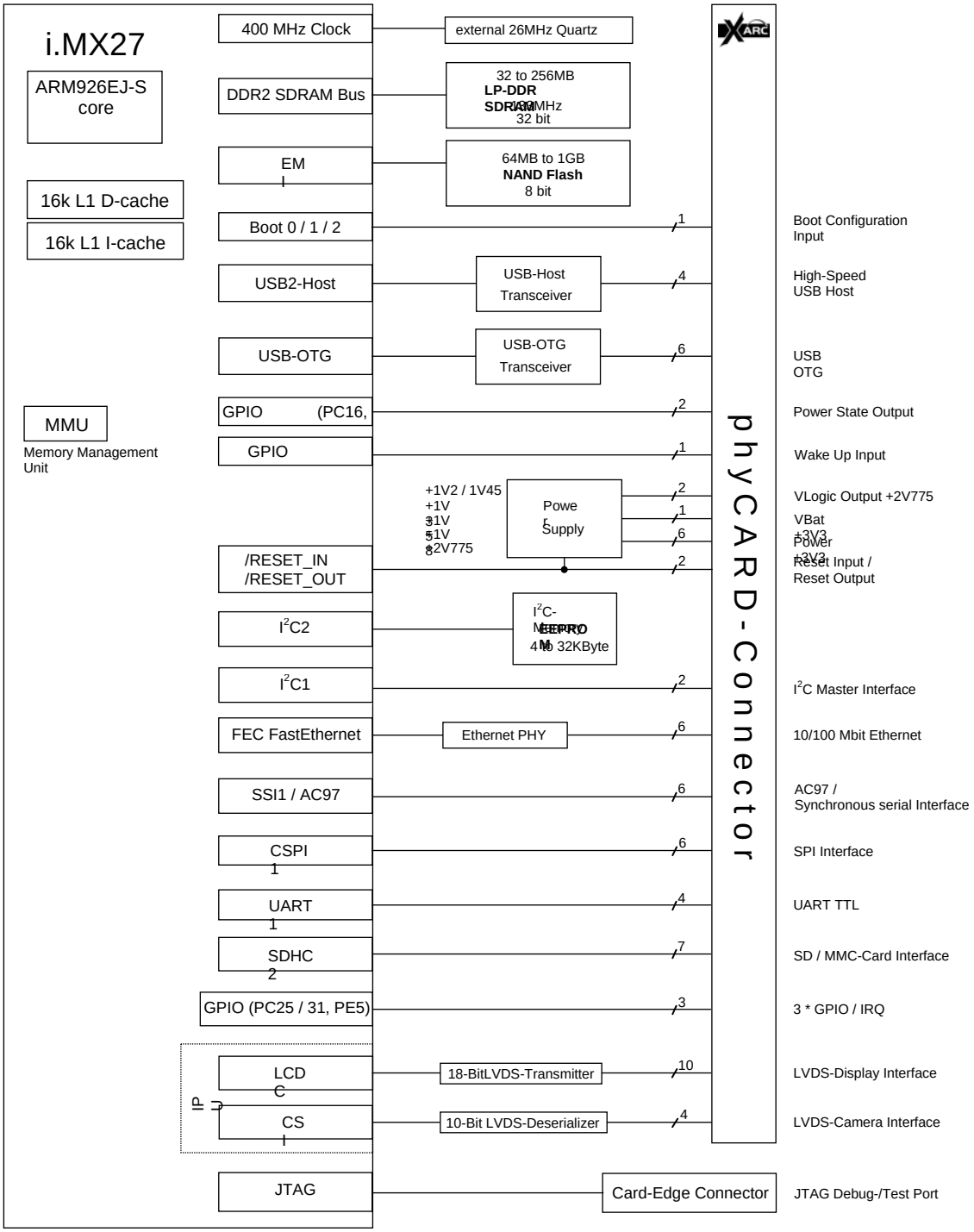

Figure 1: Block Diagram of the phyCARD-S

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1.2 View of the phyCARD-S

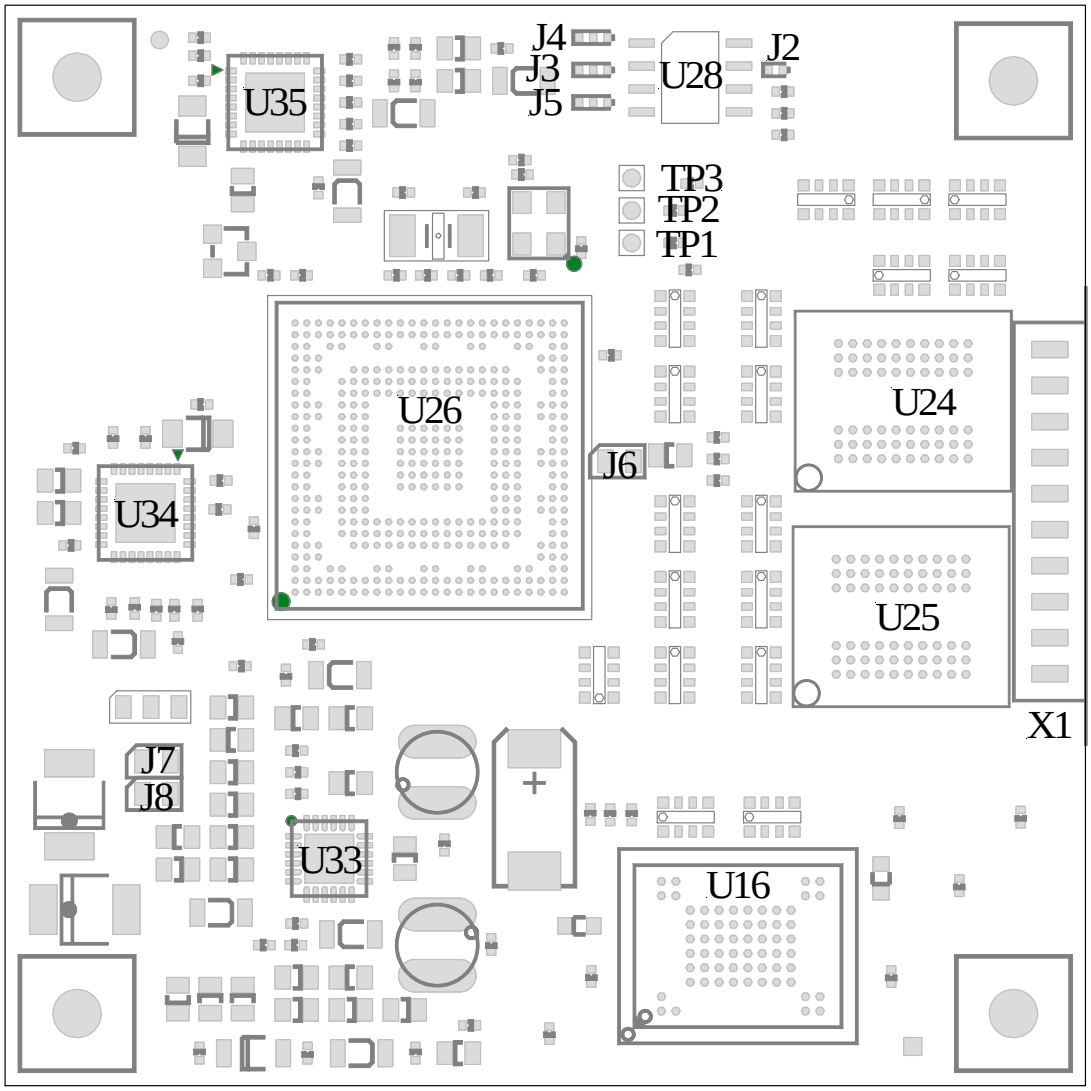

Figure 2: Top view of the phyCARD-S (controller side)

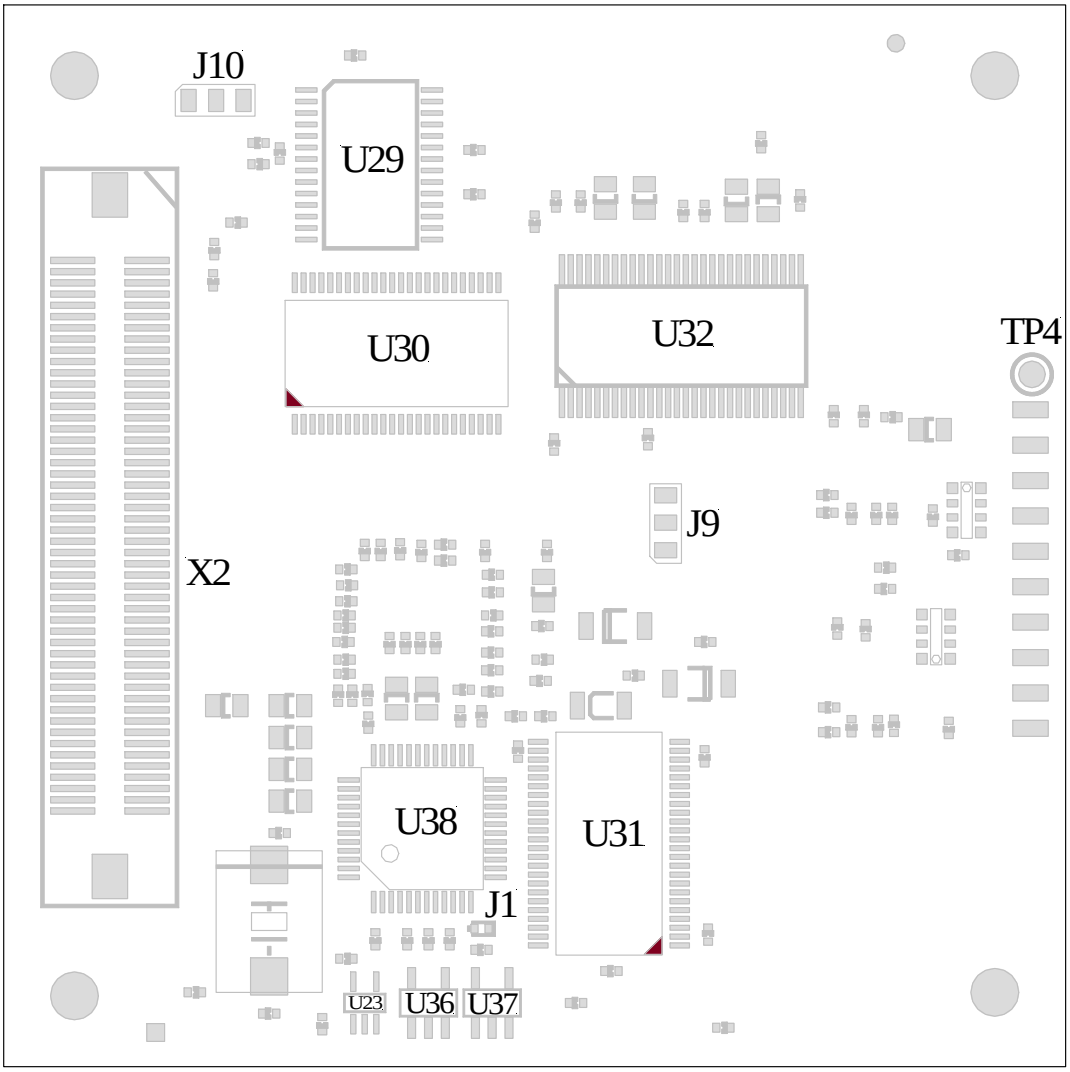

Figure 3: Bottom view of the phyCARD-S (connector side)

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1.3 Minimum Requirements to Operate the phyCARD-S

Basic operation of the phyCARD-S only requires supply of a +3V3 input voltage with 1.0 A load and the corresponding GND connection.

These supply pins are located at the phyCARD-Connector X2:

VCC_3V3: X2 1A, 2A, 3A, 1B, 2B, 3B

Connect all +3.3V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X2 4A, 8A, 13A, 4B, 8B, 13B

Please refer to section 2 for information on additional GND Pins located at the phyCARD-Connector X2

Caution:
We recommend connecting all available +3V3 input pins to the power supply system on a custom carrier board housing the phyCARD-S and at least the matching number of GND pins neighboring the +3V3 pins.

In addition, proper implementation of the phyCARD-S module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to *section 4* for more information.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all X-Arc bus signals extend to one surface mount technology (SMT) connector (0.635 mm) lining on side of the module (referred to as phyCARD-Connector). This allows the phyCARD-S to be plugged into any target application like a "big chip".

The numbering scheme for the phyCARD-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (refer to *Figure 4*).

The numbered matrix can be aligned with the phyCARD-S (viewed from above; phyCARD-Connector pointing down) or with the socket of the corresponding phyCARD Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCARD-S marked with a triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCARD-Connector as well as the mating connector on the phyBASE Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCARD-Connector is usually assigned a single designator for its position (X1 for example). In this manner the phyCARD-Connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector.

The following figure illustrates the numbered matrix system. It shows a phyCARD-S with SMT phyCARD-Connectors on its underside (defined as dotted lines) mounted on a Carrier Board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyCARD-module showing these phyCARD-Connectors mounted on the underside of the module's PCB.

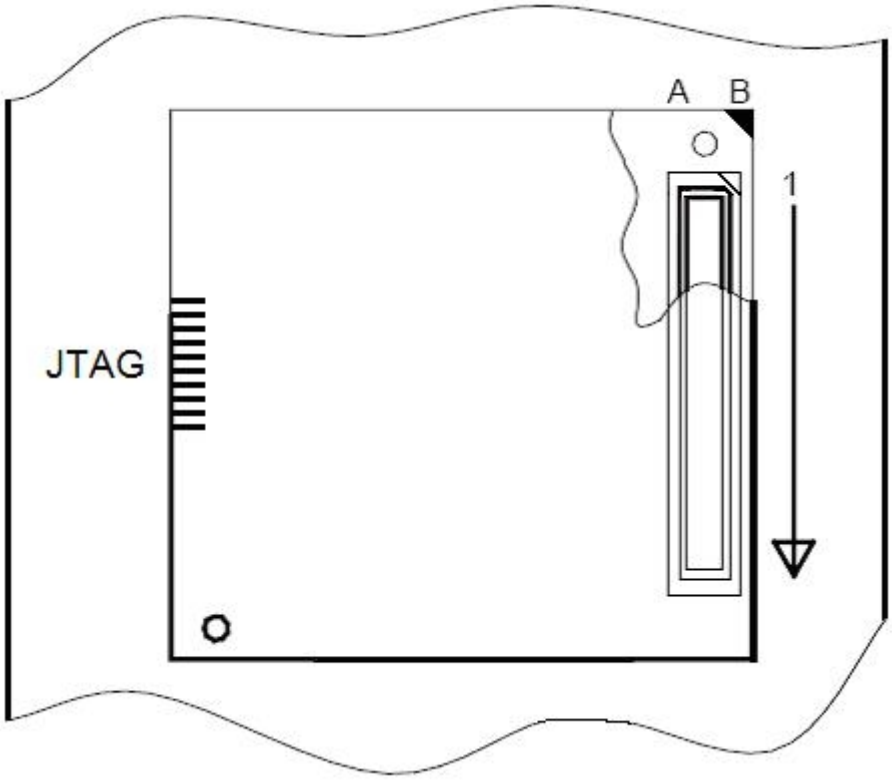


Figure 4: Pin-out of the phyCARD-Connector (top view, with cross section insert)

Table 2 shows the Pin-out of the X-Arc bus with the functional grouping of the signals, while *Table 3* provides an overview of the Pin-out of the phyCARD-Connector with signal names and descriptions specific to the phyCARD-S. It also provides the appropriate signal level interface voltages listed in the SL (**S**ignal **L**evel) column and the signal direction.

The Freescale i.MX27 is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *Freescale i.MX27 Reference Manual* for details on the functions and features of controller signals and port pins.

	I/O	Signal	Pin		Pin	Signal	I/O	
Supply	In	VCC	1A		1B	VCC	In	Supply
	In	VCC	2A		2B	VCC	In	
	In	VCC	3A		3B	VCC	In	
	In	GND	4A		4B	GND	In	
	Out	VCC_LOGIC	5A		5B	VCC_LOGIC	Out	
	-	FEEDBACK	6A		6B	VSTBY	In	
	In	nRESET_IN	7A		7B	nRESET_OUT	Out	
	-	GND	8A		8B	GND	-	
Display	Out	LVDS_TX0+	9A		9B	LVDS_TX1+	Out	Display
	Out	LVDS_TX0-	10A		10B	LVDS_TX1-	Out	
	Out	LVDS_TX2+	11A		11B	LVDS_TX3+	Out	
	Out	LVDS_TX2-	12A		12B	LVDS_TX3-	Out	
	-	GND	13A		13B	GND	-	
	Out	LVDS_TXCLK+	14A		14B	LVDS_CAM_RX+	In	Camera
	Out	LVDS_TXCLK-	15A		15B	LVDS_CAM_RX-	In	
Camera	Out	LVDS_CAM_MCLK	16A		16B	LVDS_CAM_nLOCK	Out	
I^2C		I2C_CLK	17A		17B	I2C_DATA		I^2C
	-	GND	18A		18B	GND	-	
Ethernet	Out	ETH_SPEED	19A		19B	ETH_LINK	Out	Ethernet
	Out	ETH_TX+	20A		20B	ETH_RX+	In	
	Out	ETH_TX-	21A		21B	ETH_RX-	In	
	-	GND	22A		22B	GND	-	
USB OTG	Out	USB_OTG_PWR1	23A		23B	USB_PWR2	Out	USB Host
	In	USB_OTG_OC1	24A		24B	USB_OC2	In	
	-	GND	25A		25B	GND	-	
	Bi	USB_OTG_VBUS1	26A		26B	nSuspend_to_RAM	Out	
	Bi	USB_OTG_D1-	27A		27B	USB_D2-	Bi	USB Host
	Bi	USB_OTG_D1+	28A		28B	USB_D2+	Bi	
	In	USB_OTG_UID1	29A		29B	nPower_Off	Out	
	-	GND	30A		30B	GND	-	
SD/MMC	Bi	SDIO_D0	31A		31B	SDIO_D1	Bi	SD/MMC
	Bi	SDIO_D2	32A		32B	SDIO_D3	Bi	
	Out	SDIO_CLK	33A		33B	SDIO_CMD	Bi	
	-	GND	34A		34B	GND	-	
SPI	Out	SPI_CS0	35A		35B	SPI_CS1	Out	SPI
	In	SPI_RDY	36A		36B	SPI_MOSI	Out	
	Out	SPI_CLK	37A		37B	SPI_MISO	In	
	-	GND	38A		38B	GND	-	
UART	Out	UART_TXD	39A		39B	UART_RXD	In	UART
	In	UART_RTS	40A		40B	UART_CTS	Out	
	-	GND	41A		41B	GND	-	
AC97/HDA	Bi	HDA_SEL/AC97_INT	42A		42B	AC97/HDA_BIT_CLK	Bi	AC97/HDA
	Out	AC97/HDA_SDATA_OUT	43A		43B	AC97/HDA_SYNC	Out	
	In	AC97/HDA_SDATA_IN	44A		44B	AC97/HDA_nRESET	Out	
	-	GND	45A		45B	GND	-	
GPIO	Bi	GPIO0/IRQ/PWM	46A		46B	SDIO_CD	In	SD/MMC
	Bi	GPIO2/IRQ	47A		47B	GPIO1/IRQ	Bi	GPIO
	In	nWKUP	48A		48B	for internal use only	Bi	
	-	GND	49A		49B	GND	-	
Boot Opt.	In	CONFIG0	50A		50B	CONFIG1	In	Boot Opt.

Table 2: X-Arc Bus Pin-out

Note:
SL is short for Signal Level (V) and is the applicable logic level to interface a given pin.
Those pins marked as "N/A" have a range of applicable values that constitute proper operation.

Please refer to the phyCARD Design-In Guide (LAN-051) for layout recommendations and example circuitry.

Pin Row X2A				
Pin #	Signal	I/O	SL	Description
1A	VCC_3V3	I	Power	3.3V Primary Voltage Supply Input
2A	VCC_3V3	I	Power	3.3V Primary Voltage Supply Input
3A	VCC_3V3	I	Power	3.3V Primary Voltage Supply Input
4A	GND	-	-	Ground 0V
5A	NVDD7_12_14	O	VCC_LOGIC	VCC Logic Output
6A	VCC_FEEDBACK	O	Power	Feedback Output to indicate the supply voltage required (3V3 or 5V)
7A	X_#RESET	I	VCC3V3	Active low Reset In
8A	GND	-	-	Ground 0V
9A	TXOUT0+	O	LVDS	LVDS Chanel 0 positive Output
10A	TXOUT0-	O	LVDS	LVDS Chanel 0 negative Output
11A	TXOUT2+	O	LVDS	LVDS Chanel 2 positive Output
12A	TXOUT2-	O	LVDS	LVDS Chanel 2 negative Output
13A	GND	-	-	Ground 0V
14A	TXCLKOUT+	O	LVDS	LVDS Clock positive Output
15A	TXCLKOUT-	O	LVDS	LVDS Clock negative output
16A	X_CSI_MCLK	O	VCC_LOGIC	Clock Output for Camera Interface
17A	X_I2C_CLK	O	VCC_LOGIC	I2C Clock Output
18A	GND	-	-	Ground 0V
19A	X_ETH_SPEED	O	VCC3V3	Ethernet Speed Indicator (Open Drain)
20A	X_ETH_TX+	O (I)	VCC3V3	Transmit positive output (normal) Receive positive input (reversed)
21A	X_ETH_TX-	O (I)	VCC3V3	Transmit negative output (normal) Receive negative input (reversed)
22A	GND	-	-	Ground 0V
23A	X_USB_HS_/PSW	O	VCC3V3	USB-OTG Power switch output open drain
24A	X_USB_HS_FAULT	I	VCC3V3	USB-OTG over current input signal
25A	GND	-	0	Ground 0V

26A	X_VBUS	I	5V	USB VBUS Voltage
27A	X_UDM	I/O		USB transceiver cable interface, D-
28A	X_UDP	I/O		USB transceiver cable interface, D+
29A	X_UID	I		USB on the go transceiver cable ID resistor connection
30A	GND	-	0	Ground 0V
31A	X_SD2_D0	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
32A	X_SD2_D2	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
33A	X_SD2_CLK	O	VCC_LOGIC	SD/MMC Clock for MMC/SD/SDIO
34A	GND	-	-	Ground 0V
35A	X_CSPI1_SS0	O	VCC_LOGIC	SPI 1 Chip select 0
36A	X_#CSPI1_RDY	O	VCC_LOGIC	SPI 1 SPI data ready in Master mode
37A	X_CSPI1_SCLK	O	VCC_LOGIC	SPI 1 clock
38A	GND	-	-	Ground 0V
39A	UART1_TXD	O	VCC_LOGIC	Serial transmit signal UART 1
40A	UART1_RTS	O	VCC_LOGIC	Request to send UART 1
41A	GND	-	-	Ground 0V
42A	HAD_SEL/AC_INT	I/O-	VCC_LOGIC	AC97 Interrupt Input
43A	SSI1_TXDAT	O	VCC_LOGIC	AC97 Transmit Output
44A	SSI1_RXDAT	I	VCC_LOGIC	AC97 Receive Input
45A	GND	-	-	Ground 0V
46A	GPIO0_IRQ	I/O	VCC_LOGIC	GPIO0 (µC port PC31)
47A	GPIO2_IRQ	I/O	VCC_LOGIC	GPIO2 (µC port PE5)
48A	X_WAKEUP	I	VCC3V3	Wakeup Interrupt Input (µC port PC15)
49A	GND	-	-	Ground 0V
50A	X_BOOT1	I	-	Boot-Mode Input

PIN ROW X2B				
PIN #	SIGNAL	I/O	SL	DESCRIPTION
1B	VCC_3V3	-	Power	3.3V Primary Voltage Supply Input
2B	VCC_3V3	-	Power	3.3V Primary Voltage Supply Input
3B	VCC_3V3	-	Power	3.3V Primary Voltage Supply Input
4B	GND	-	-	Ground 0V
5B	NVDD7_12_14	O	VCC_LOGIC	Display vertical synchronization pulse
6B	VBAT	-	Power	Standby Voltage Input
7B	X_#RESET_OUT	-	VCC_LOGIC	Active low Reset output
8B	GND	-	-	Ground 0V
9B	TXOUT1+	O	LVDS	LVDS Chanel 0 positive Output
10B	TXOUT1-	O	LVDS	LVDS Chanel 0 negative Output
11B	TXOUT3+	O	LVDS	LVDS Chanel 3 positive Output
12B	TXOUT3-	O	LVDS	LVDS Chanel 3 negative Output
13B	GND	-	-	Ground 0V
14B	RXIN+	O	LVDS	LVDS Receive positive Input for Camera
15B	RXIN-	O	LVDS	LVDS Receive negative Input for Camera
16B	LOCK	O	VCC_LOGIC	Lock Output for Camera Interface
17B	X_I2C_DATA	I/O	VCC_LOGIC	I2C Data
18B	GND	-	-	Ground 0V
19B	X_ETH_LINK	O	VCC3V3	Ethernet Speed Indicator (Open Drain)
20B	X_ETH_RX+	I (O)	VCC3V3	Receive positive input (normal) Transmit positive output (reversed)
21B	X_ETH_RX-	I (O)	VCC3V3	Receive negative input (normal) Transmit negative output (reversed)
22B	GND	-	-	Ground 0V
23B	X_USB_HS_/PSW2	O	VCC_LOGIC	USB-HOST Power switch output open drain
24B	X_USB_HS_FAULT2	I	VCC_LOGIC	USB-HOST over current input signal
25B	GND	-	-	Ground 0V
26B	X_#SUSP_RAM	OC	VCC_LOGIC	Suspend to RAM Open Collector Output (µC port PC16)
27B	X_UDM2	I/O		USB HOST transceiver cable interface, D-
28B	X_UDP2	I/O		USB HOST transceiver cable interface, D+
29B	X_#PWR_OFF	OC	VCC_LOGIC	Power Off Open Collector Output (µC port PC17)
30B	GND	-	-	Ground 0V

31B	X_SD2_D1	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
32B	X_SD2_D3	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
33B	X_SD2_CMD	O	VCC_LOGIC	SD/MMC Command for MMC/SD/SDIO
34B	GND	-	-	Ground 0V
35B	X_CSPI1_SS1	O	VCC_LOGIC	SPI 1 Chip select 1
36B	X_CSPI1_MOSI	I/O	VCC_LOGIC	SPI 1 Master data out; slave data in
37B	X_CSPI1_MISO	I/O	VCC_LOGIC	SPI 1 Master data in; slave data out
38B	GND	-	-	Ground 0V
39B	UART1_RXD	I	VCC_LOGIC	Serial data receive signal UART 1
40B	UART1_CTS	I	VCC_LOGIC	Clear to send UART 1
41B	GND	-	-	Ground 0V
42B	SSI1_CLK	I	VCC_LOGIC	AC97 Clock
43B	SSI1_FS	O	VCC_LOGIC	AC97 SYNC
44B	SSI1_RES	O	VCC_LOGIC	AC97 Reset
45B	GND	-	-	Ground 0V
46B	X_SD2_CD	I	VCC_LOGIC	SD/MMC Card Detect for MMC/SD/SDIO
47B	GPIO1_IRQ	I/O	VCC_LOGIC	GPIO1 (µC port PC25)
48B	X_ONEWIRE	-	VCC_LOGIC	Hardware Introspection Interface for internal use only
49B	GND	-	-	Ground 0V
50B	Not connected	-	-	Pin left unconnected

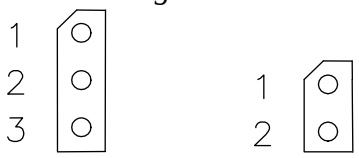
Table 3: Pin-out of the phyCARD-Connector X2

3 Jumpers

For configuration purposes, the phyCARD-S has 11 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location of the solder jumpers on the board. 7 solder jumpers are located on the top side of the module (opposite side of connectors) and 3 solder jumpers are located on the bottom side of the module (connector side). *Table 4* below provides a functional summary of the solder jumpers which can be changed to adapt the phyCARD-S to your needs. It shows their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable chapter listed in the table.

Note:
Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyCARD-S.

Figure 5: Typical jumper pad numbering scheme



e.g.: e.g.:

If manual jumper modification is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Please pay special attention to the "TYPE" column to ensure you are using the correct type of jumper (0 Ohms, 10k Ohms, etc…). The jumpers are either 0805 package or 0402 package with a 1/8W or better power rating.

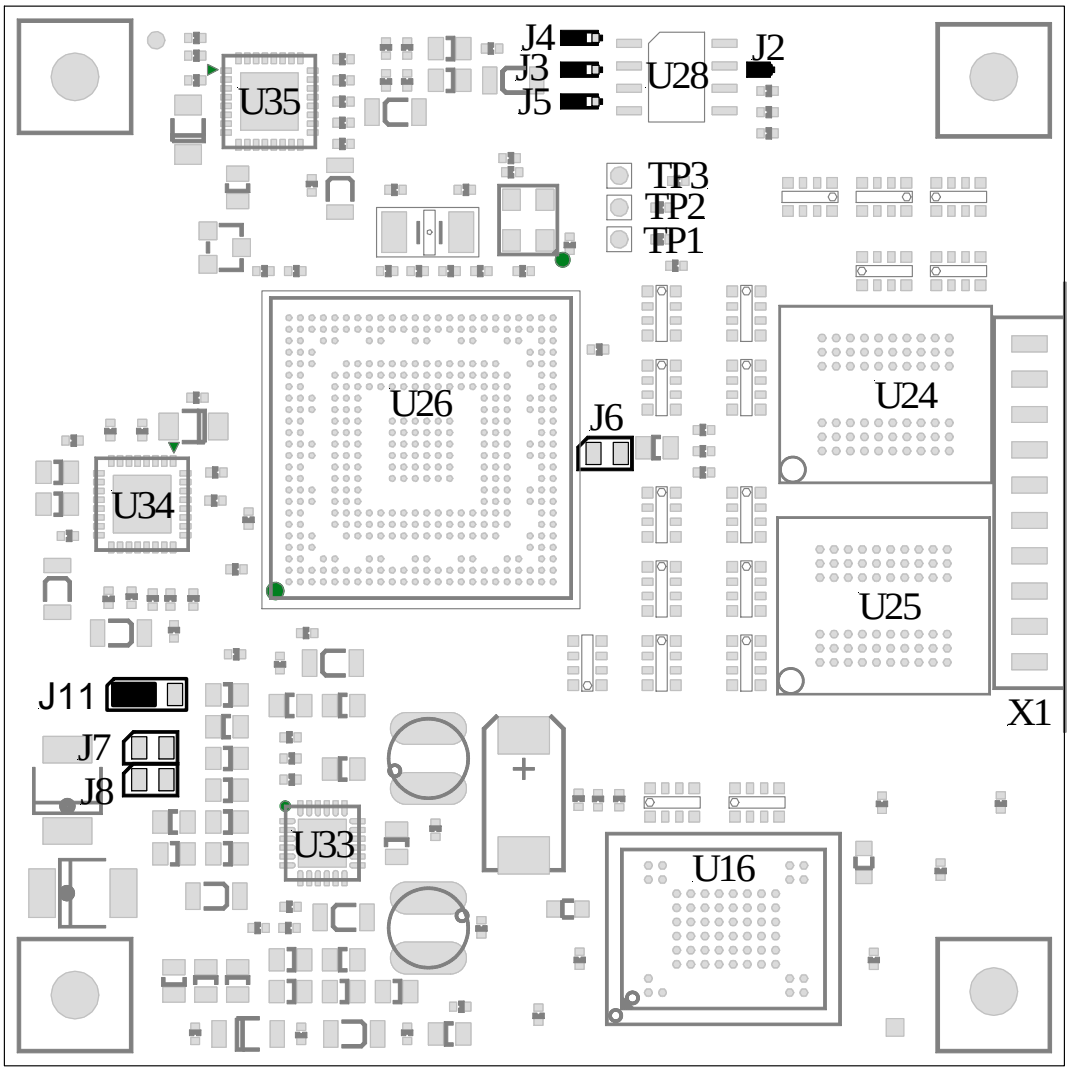


Figure 6: Jumper locations (top view)

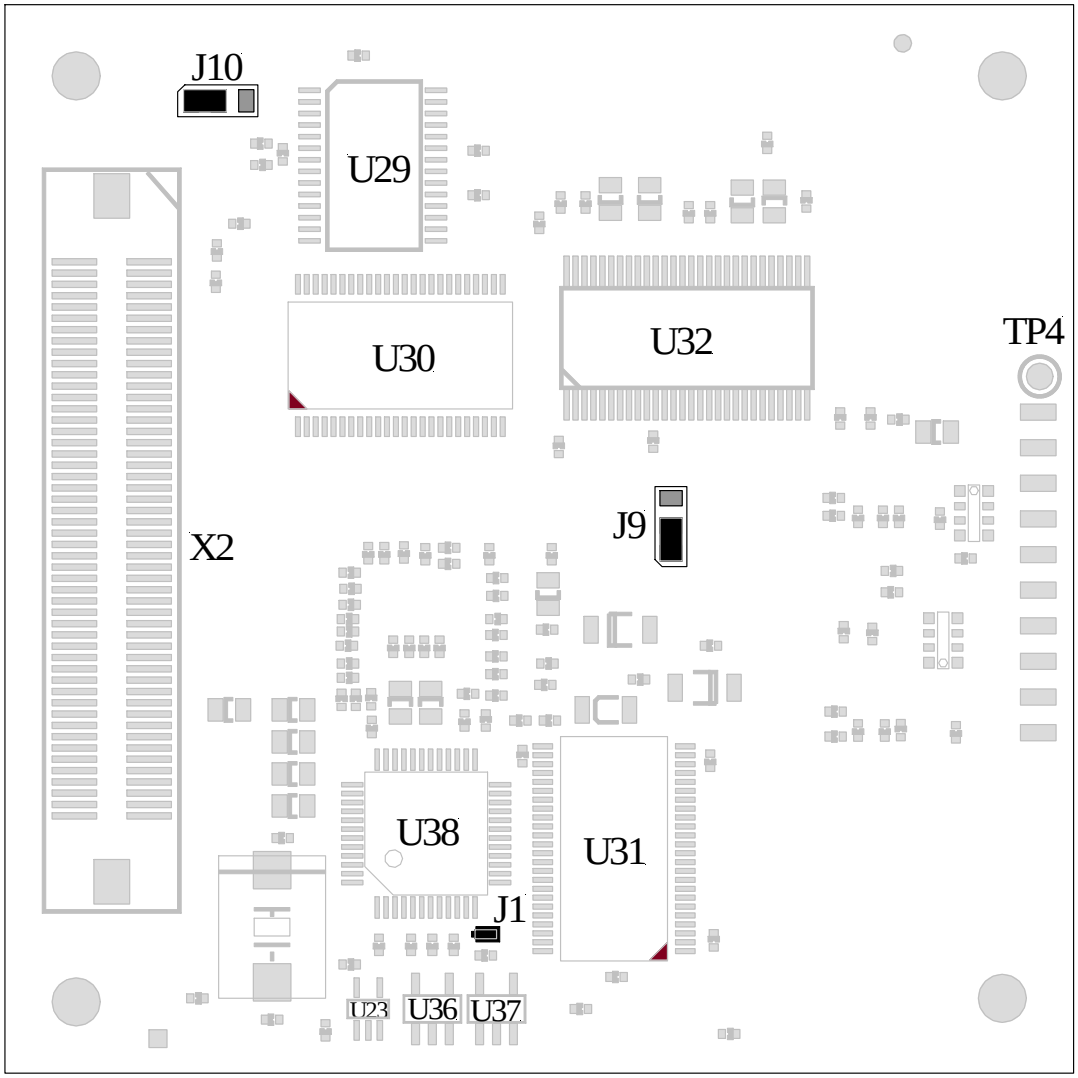


Figure 7: Jumper locations (bottom view)

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The jumpers (J = solder jumper) have the following functions:

Jumper	Description	Type	Chapter
J1	J1 connects the reset input of the Ethernet PHY (U38) with GPIO PC30. Thereby it is possible to perform a reset of the Ehernet PHY, not only by hardware, but also by software.	0R (0402)	*9.4.2*
open	Software reset of the Ethernet PHY disabled		
closed	**Software reset of the Ethernet PHY possible via GPIO PC30**		
J2	J2 connects pin 7 of the serial memory at U28 to GND. On many memory devices pin 7 enables/disables the activation of a write protect function. It is not guaranteed that the standard serial memory populating the phyCARD-S will have this write protection function. *Please refer to the corresponding memory data sheet for more detailed information.*	0R (0402)	*7.3.2*
open	EEPROM U28 is write protected		
closed	**EEPROM U28 is not write protected**		
J4, J3, J5	J4, J3 and J5 define the slave addresses (A0 toA2) of the serial memory U28 on the I^2C2 bus. In the high-nibble of the address, I^2C memory devices have the slave ID 0xA. The low-nibble is build from A2, A1, A0, and the R/W bit. .	0R (0402)	*7.3.1*
all 2+3	**A0 = 0, A1 = 1, A2= 0, => 0x2 is selected as the low-nibble of the EEPROM's address**		
other settings	please refer to *Table 9* to find alternative addresses resulting from other combinations of jumpers J3, J4, and J5		
J6	J6 allows to attach a programming voltage to the IC Identification Module (IIM) for programming and/or overriding identification and control information stored in on-chip fuse elements.	0R (0805)	
open	**VDD_FUSE not connected**		
closed	**Only close Jumper when burning of fuses is required**		

Jumper	Description	Type	Chapter
J9	J9 selects rising, or falling edge strobe for the LVDS Transmitter at U32 used for the display connectivity of the phyCARD-S.	10k (0805)	*12.1*
1+2	**rising edge strobe used for the LVDS display signals**		
2+3	falling edge strobe used for the LVDS display signals		
J10	J10 selects rising, or falling edge strobe for the LVDS Deserializer at U29 used for the display connectivity of the phyCARD-S	10k (0805)	*13.1*
1+2	**rising edge strobe used for the LVDS camera signals**		
2+3	falling edge strobe used for the LVDS camera signals		
J11	J11 selects either signal OE_ACD, or PS as data enable of the display interface	0R (0805)	*12.1*
1+2	**OE_ACD used as data enable**		
2+3	PS used as data enable		

Table 4: Jumper settings

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4 Power

The phyCARD-S operates off of a single power supply voltage.

The following sections of this chapter discuss the primary power pins on the phyCARD-Connector X2 in detail.

4.1 Primary System Power (VCC_3V3)

The phyCARD-S operates off of a primary voltage supply with a nominal value of +3.3V. On-board switching regulators generate the 1.3V, 1.45V, 1,5V, 1.8V, and 2.775V voltage supplies required by the i.MX27 MCU and on-board components from the primary 3.3V supplied to the SBC.

For proper operation the phyCARD-S must be supplied with a voltage source of 3.3V ±5 % with 1.0 A load at the VCC pins on the phyCARD-Connector X2.

VCC_3V3: X2 1A, 2A, 3A, 1B, 2B, 3B

Connect all +3.3V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X2 4A, 8A, 13A, 4B, 8B, 13B

Please refer to *section 1* for information on additional GND Pins located at the phyCARD-Connector X2.

Caution:
As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance all GND pins should be connected to a solid ground plane.

4.2 Standby Voltage (VBAT)

For applications requiring a standby mode a secondary voltage source of 3.3V can be attached to the phyCARD-S at pin X2B6. This voltage source is supplying the core and on-chip peripherals of the i.MX27 (e.g. RTC, PLL, etc.), as well as the SDRAM and NAND Flash memory while the primary system power (VCC_3V3) is removed. Applications not requiring a standby mode can connect the VBAT pin to the primary system power supply (VCC = 3.3V), or can leave it open.

4.3 On-board Voltage Regulator (U33)

The phyCARD-S provides an on-board switching regulator (U33) to source the five different voltages (1.3V, 1.45V, 1.5V, 1.8V, and 2.775V) required by the processor and on-board components.
Figure 8 presents a graphical depiction of the powering scheme.

The switching regulator has two input voltage rails as can be seen in *Figure 8*. 3V3 and 3V3 Backup. 3V3 is supplied from the primary voltage input pins VCC_3V3 of the phyCARD-S, whereas 3V3 Backup is supplied from the primary voltage input pins (VCC_3V3) and the secondary voltage input pin VBAT. Not all devices on the phyCARD-S are supplied from the switching regulator. Some, such as the Ethernet PHY, the LVDS Transmitter, etc. are directly connected to the primary voltage input pins VCC_3V3. The following list summarizes the relation between the different voltage rails and the devices on the phyCRAD-S:

External voltages: VCC_3V3 and VBAT (optional)

- VCC_3V3: 3V3 Voltage Regulator, Ethernet PHY, LVDS Transmitter , LVDS Deserializer
- VBAT: 3V3 BACKUP Voltage Regulator

Internally generated voltages: 1V3, 1V45, 1V5, 1V8 and 2V775

- 1V3 on-chip RTC of the i.MX27 (RTCVDD) and 32kHz oscillator (OSC32VDD)
- 1V45 i.MX27 core (QVDD)
- 1V5 on-chip PLLs
- 1V8 AVDD, NVDD1_2_3_4_5 and NVDD13 of the i.MX27, DDR SDRAM, NAND Flash
- 2V775 NVDD6_8_9_10, NVDD7_12_14, NVDD15 and 26MHz oscillator of the i.MX27, USB-Transceiver, I^2C EEPROM

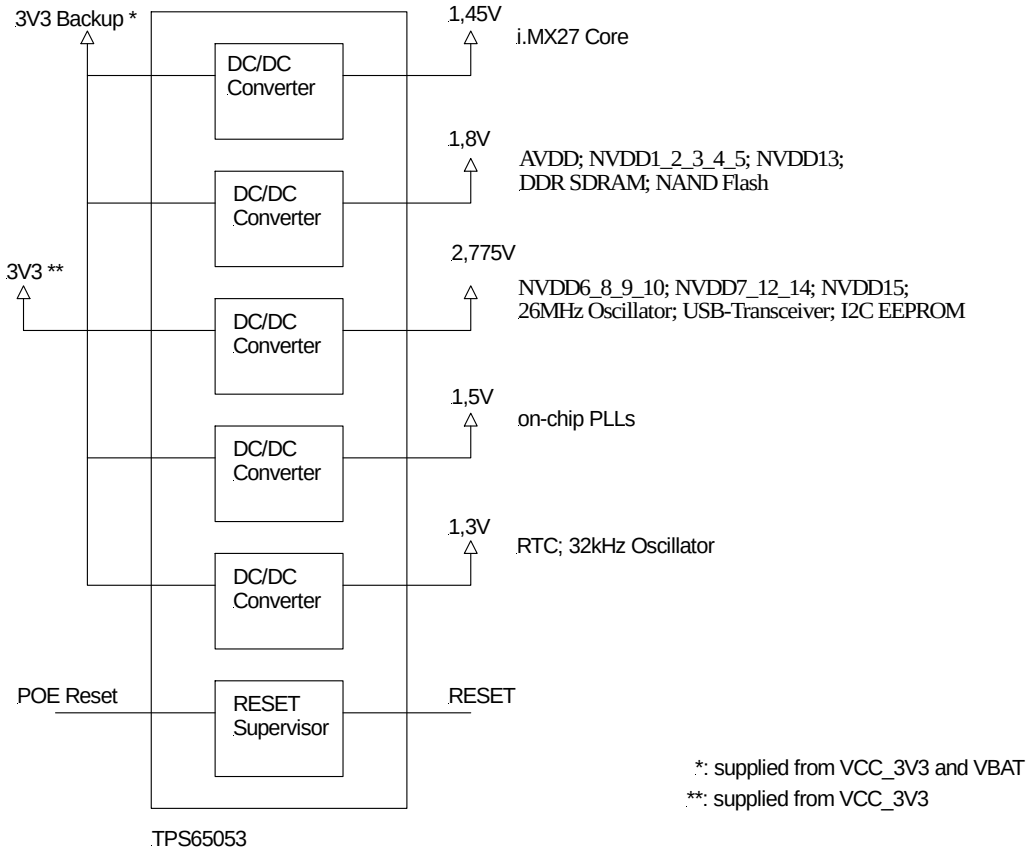

Figure 8: Power Supply Diagram

4.4 Supply Voltage for external Logic

The voltage level of the phyCARDs logic circuitry is VCC_LOGIC (2.775V) which is generated on-board. In order to allow connecting external devices to the phyCARD-S without the need of another voltage source in addition to the primary supply this voltage is brought out at pins X2A5 and X2B5 of the phyCARD-Connector.

Use of level shifters supplied with VCC_LOGIC allows converting the signals according to the needs on the custom target hardware. Alternatively signals can be connected to an open drain circuitry with a pull-up resistor attached to VCC_LOGIC.

5 Power Management

The phyCARD-S was designed to support applications requiring a power management. Three pins of the X-Arc bus are designated for this purpose. X_#PWR_OFF and X_#SUSP_RAM are output pins which can be used to indicate the power status of the phyCARD-S, whereas X_WAKEUP is an input pin to apply a wake up signal to the phyCARD-S.

All three pins lead to GPIOs of the i.MX. Thus their functionality can be programmed to your needs.

The following table shows the location of the power management pins on the phyCARD-Connector and the corresponding GPIOs of the i.MX27.

Pin #	Signal	I/O	SL	Description
48A	X_WAKEUP	I	VCC3V3	Wakeup Interrupt Input (µC port PC15)
26B	X_#SUSP_RAM	OC	VCC_LOGIC	Suspend to RAM Open Collector Output (µC port PC16)
29B	X_#PWR_OFF	OC	VCC_LOGIC	Power Off Open Collector Output (µC port PC17)

Table 5: Power Management Pins

With the two output signals nPower_Off (pin X_#PWR_OFF) and nSuspend_to_RAM (pin X_#SUSP_RAM) three different power states can be defined.

Power State / Signal	Power On	Standby	Off
nSuspend_to_RAM	High	Low	X
nPower_Off	High	High	Low
VCC_3V3	On	Off	Off
VBAT	X	On	Off

X=don't care

Table 6: Power States

Please refer to the chapter "Power Management" in the phyCARD Design-In Guide for more information about the implementation of the power management into your design.

Caution:
According to the specification for the phyCARD family writing custom software to utilize pins X_#SUSP_RAM and X_#PWR_OFF requires them to be configured as Open Collector Output.

6 System Configuration and Booting

Although most features of the i.MX27 microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

The system start-up configuration includes:

- Clock/PLL configuration
- Boot device select configuration
- NAND Flash configuration

During the reset cycle the operational system boot mode of the i.MX27 processor is determined by the configuration of the four external input pins, BOOT[3:0]. The settings of these pins control where the system is boot from and the memory port size.

The following table shows the different boot modes, which can be selected by configuring the four external input pins, BOOT[3:0] of the i.MX27. Please note that only the ones in bold letters are applicable for the phyCARD-S.

Boot Mode Selection BOOT[3:0]	Boot Mode/Device
0000	**Bootstrap from UART/USB**
0001	Reserved
0010	**8-bit NAND Flash (2 Kbyte per page)**
0011	16-bit NAND Flash (2 Kbyte per page)
0100	16-bit NAND Flash (512 bytes per page)
0101	16-bit CS0 (NOR-Flash)
0110	32-bit CS0
0111	**8 bit NAND Flash (512 bytes per page)**
1xxx	Reserved

Table 7: Boot Modes of i.MX27 module

The i.MX27 processor always begins fetching instruction from the address 0x00000000 after reset. The BOOT[3:0] pins control the memory region that is mapped to the address 0x0 as shown in *Table* 7. These boot modes information are registered during the system reset. When an external chip select is enabled by the BOOT[3:0] pins, the reset vector 0x0 will jump to the corresponding boot address space.

The standard phyCARD-S module with 64MB NAND Flash comes with a boot configuration of **'0111'**, so the system will boot from the 8-bit NAND Flash at CS0, the phyCARD-S module with more than 128MB NAND flash comes with a boot configuration of **'0010'**.

The configuration circuitry (pull-up or pull-down resistors) are located on the phyCARD module. They are already set for booting from the NAND Flash, so no further settings are necessary.

The boot mode input (X2A50: X_BOOT1) allows for starting the bootstrap program residing in the internal ROM of the i.MX27 rather than booting from NAND Flash without modifying the circuitries on the phyCARD-S. In order to start the bootstrap program a low level must be applied to the boot mode input.

7 System Memory

The phyCARD-S provides three types of on-board memory:

- LP-DDR-SDRAM: 32MByte (up to 256MByte)
- NAND Flash: 128MByte (up to 1GByte)
- I²C-EEPROM: 4KB (up to 32KByte)

The following sections of this chapter detail each memory type used on the phyCARD-S.

7.1 LP-DDR-SDRAM (U24, U25)

The RAM memory of the phyCARD-S in comprised of two 16-bit wide LP-DDR-SDRAM chips at U24 and U25. They are connected to the special SDRAM interface of the i.MX27 processor, configured for 32-bit access, and operating at the maximum frequency of 133MHz.

The SDRAM memory is accessed via the second AHB port using chip select signal /CSD0 (/CS2) starting at 0xA000 0000.

Typically the LP-DDR-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the i.MX27 controller. Refer to the i.MX27 Reference Manual for accessing and configuring these registers.

7.2 NAND Flash Memory (U16)

Use of Flash as non-volatile memory on the phyCARD-S provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyCARD-S:

Manufacturer	NAND Flash P/N	Density (MByte)
ST Microelectronics	NAND01GR3B2CZA6E	128

Table 8: Compatible NAND Flash devices

Additionally, any parts that are footprint (VFBGA) and functionally compatible with the NAND Flash devices listed above may also be used with the phyCARD-S.

These Flash devices are programmable with 1.8 V. No dedicated programming voltage is required.

As of the printing of this manual these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

The NAND Flash memory is connected to the NF bus. This chip select signal is used for boot operation.

7.3 I²C EEPROM (U28)

The phyCARD-S is populated with a ST 24W32C[1] non-volatile 4KByte EEPROM with an I²C interface at U28. This memory can be used to store configuration data or other general purpose data. This device is accessed through I²C port 2 on the i.MX27. The control registers for I²C port 2 are mapped between addresses 0x1001 D000

1: See the manufacturer's data sheet for interfacing and operation.

and 0x1001 DFFF. Please see the *i.MX27 Reference* Manual for detailed information on the registers.

Three solder jumpers are provided to set the lower address bits: J3, J4 and J5. Refer to *section 7.3.1* for details on setting these jumpers.

Write protection to the device is accomplished via jumper J2. Refer to *section 7.3.2* for further details on setting this jumper.

7.3.1 Setting the EEPROM Lower Address Bits (J3, J4, J5)

The 32KB I²C EEPROM populating U28 on the phyCARD-S module has the capability of configuring the lower address bits A0, A1, and A2. The four upper address bits of the device are fixed at '1010' (*see ST 24W32C data sheet).* The remaining three lower address bits of the seven bit I²C device address are configurable using jumpers J3, J4 and J5. J4 sets address bit A0, J3 address bit A1, and J5 address bit A2.

Table 9 below shows the resulting seven bit I²C device address for the eight possible jumper configurations.

U28 I²C Device Address	J5	J3	J4
1010 010	**2 + 3**	**2 + 3**	**2 + 3**
1010 011	2 + 3	2 + 3	1 + 2
1010 000	2 + 3	1 + 2	2 + 3
1010 001	2 + 3	1 + 2	1 + 2
1010 110	1 + 2	2 + 3	2 + 3
1010 111	1 + 2	2 + 3	1 + 2
1010 100	1 + 2	1 + 2	2 + 3
1010 101	1 + 2	1 + 2	1 + 2

Table 9: U28 EEPROM I²C address via J3, J4, and J5[1]

[1]: Defaults are in **bold blue** text

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7.3.2 EEPROM Write Protection Control (J2)

Jumper J2 controls write access to the EEPROM (U28) device. Closing this jumper allows write access to the device, while removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device.

The following configurations are possible:

EEPROM Write Protection State	J2
Write access allowed	**closed**
Write protected	open

Table 10: EEPROM write protection states via J2[1]

7.4 Memory Model

There is no special address decoding device on the phyCARD-S, which means that the memory model is given according to the memory mapping of the i.MX27. Please refer to the *i.MX27 Reference Manual* for more information on the memory mapping.

1: Defaults are in **bold blue** text

8 SD / MMC Card Interfaces

The X-Arc bus features an SD / MMC Card interface. On the phyCARD-S the interface signals extend from the controllers second Secure Digital Host Controller (SD2) to the phyCARD-Connector. *Table 11* shows the location of the different interface signals on the phyCARD-Connector. The Secure Digital Host Controller is fully compatible with the SD Memory Card Specification 1.0 and SD I/O Specification 1.0 with 1 and 4 channel(s) and supports data rates from 25 Mbps to 100 Mbps (refer to the *i.MX27 Reference Manual* for more information).

Due to compatibility reasons a card detect signal (X_SD2_CD) is added to the SD / MMC Card Interface. This signal connects to port PC29 of the i.MX27.

Pin #	Signal	I/O	SL	Description
X2A31	X_SD2_D0	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
X2A32	X_SD2_D2	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
X2A33	X_SD2_CLK	O	VCC_LOGIC	SD/MMC Clock for MMC/SD/SDIO
X2B31	X_SD2_D1	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
X2B32	X_SD2_D3	I/O	VCC_LOGIC	SD/MMC Data line both in 1-bit and 4-bit mode
X2B33	X_SD2_CMD	O	VCC_LOGIC	SD/MMC Command for MMC/SD/SDIO
X2B46	X_SD2_CD	I	VCC_LOGIC	SD/MMC Card Detect for MMC/SD/SDIO

Table 11: Location of SD/ MMC Card interface signals

Note:
The signal level of the SD / MMC card interface is 2.775V. Thus integration of an SD / MMC card slot on custom target hardware requires level shifters supplied with VCC_LOGIC (X2A5 and X2B5) at one of the supply rails.

Please refer to the chapter "SD / MMC" in the phyCARD Design-In Guide for more information about connecting an SD / MMC Card slot to the phyCARD-S.

9 Serial Interfaces

The phyCARD-S provides seven serial interfaces some of which are equipped with a transceiver to allow direct connection to external devices:

1. High speed UART (TTL, derived from UART1 of the i.MX27) with up to 4.125Mbit/s and hardware flow control (RTS and CTS signals)
2. High speed USB OTG transceiver supporting the i.MX27 USB OTG interface
3. High speed USB HOST transceiver supporting the i.MX27 USB Host interface
4. Auto-MDIX enabled 10/100 Ethernet PHY supporting the i.MX27 Ethernet MAC
5. I^2C interface (derived from first I^2C port of the i.MX27)
6. Serial Peripheral Interface (SPI) interface (extended from the first SPI modul of the i.MX27)
7. Synchronous Serial Interface (SSI) with AC97 support (originating from the synchronous serial interface of the i.MX27)

The following sections of this chapter detail each of these serial interfaces and any applicable configuration jumpers.

Caution:
Please pay special attention to the Signal Level (SL) column in the following tables. Some of the serial interfaces signal level is VCC_LOGIC, which is 2.775V and which is not identical with the voltage level of the primary supply voltage of the phyCARD-S. When connecting these interfaces to external devices level shifters supplied with VCC_LOGIC (X2A5 and X2B5) at one of the supply rails should be used.

Please refer to the phyCARD Design-In Guide for more information about using the serial interfaces of the phyCARD-S in customer applications.

9.1 Universal Asynchronous Interface

The phyCARD-S provides a high speed universal asynchronous interface with up to 4.125Mbit/s and hardware flow control (RTS and CTS signals). The following table shows the location of the signals on the phyCARD- Connector.

PIN #	SIGNAL	I/O	SL	DESCRIPTION
X2A39	UART1_TXD	O	VCC_LOGIC	Serial transmit signal UART 1
X2A40	UART1_RTS	O	VCC_LOGIC	Request to send UART 1
X2B39	UART1_RXD	I	VCC_LOGIC	Serial data receive signal UART 1
X2B40	UART1_CTS	I	VCC_LOGIC	Clear to send UART 1

Table 12: Location of the UART signals

The signals extend from UART1 of the i.MX27 directly to the phyCARD-Connector without conversion to RS-232 level. External RS-232 transceivers must be attached by the user if RS-232 levels are required.

9.2 USB-OTG Transceiver (U34)

The phyCARD-S is populated with an NXP ISP1504 USB On-The-Go High-Speed transceiver at U34 which is capable of high speed, full speed, and low speed data transmission. The ISP1504 functions as the transceiver for the i.MX27 USB-OTG Controller. An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyCARD-S USB OTG functionality. The applicable interface signals can be found on the phyCARD-Connector as shown in *Table 13*.

PIN #	SIGNAL	I/O	SL	DESCRIPTION
X2A23	X_USB_HS_/PSW	O	VCC3V3	USB-OTG Power switch output open drain
X2A24	X_USB_HS_FAULT	I	VCC3V3	USB-OTG over current input signal
X2A26	X_VBUS	I	5V	USB VBUS Voltage
X2A27	X_UDM	I/O		USB transceiver cable interface, D-
X2A28	X_UDP	I/O		USB transceiver cable interface, D+
X2A29	X_UID	I		USB on the go transceiver cable ID resistor connection

Table 13: Location of the USB-OTG signals

9.3 USB-Host Transceiver (U35)

The phyCARD-S is populated with a second NXP ISP1504 USB Host High-Speed transceiver (U35) supporting high speed, full speed, and low speed data rates. The ISP1504 functions as the transceiver for the second Host Controller (HOST2) of the i.MX27. An external USB Standard-A (for USB host connector is all that is needed to interface the phyCARD-S USB Host functionality. The applicable interface signals (D+/D-/ /PSW/FAULT) can be found on the phyCARD-Connector..

PIN #	SIGNAL	I/O	SL	DESCRIPTION
X2B23	X_USB_HS_/PSW2	O	VCC_LOGIC	USB-HOST Power switch output open drain
X2B24	X_USB_HS_FAULT2	I	VCC_LOGIC	USB-HOST over current input signal
X2B27	X_UDM2	I/O		USB HOST transceiver cable interface, D-
X2B28	X_UDP2	I/O		USB HOST transceiver cable interface, D+

Table 14: Location of the USB-Host signals

9.4 Ethernet Interface

Connection of the phyCARD-S to the world wide web or a local area network (LAN) is possible using the integrated FEC (Fast Ethernet Controller) of the i.MX27. The FEC operates with a data transmission speed of 10 or 100 Mbit/s.

9.4.1 PHY Physical Layer Transceiver (U38)

With a physical layer transceiver mounted at U38 the phyCARD-S has been designed for use in 10Base-T and 100Base-T networks. The 10/100Base-T interface with its LED signals extends to phyCARD-Connector X2.

PIN #	SIGNAL	I/O	SL	DESCRIPTION
X2A19	X_ETH_SPEED	O	VCC3V3	Ethernet Speed Indicator (Open Drain)
X2A20	X_ETH_TX+	O (I)	VCC3V3	Transmit positive output (normal) Receive positive input (reversed)
X2A21	X_ETH_TX-	O (I)	VCC3V3	Transmit negative output (normal) Receive negative input (reversed)
X2B19	X_ETH_LINK	O	VCC3V3	Ethernet Speed Indicator (Open Drain)
X2B20	X_ETH_RX+	I (O)	VCC3V3	Receive positive input (normal) Transmit positive output (reversed)
X2B21	X_ETH_RX-	I (O)	VCC3V3	Receive negative input (normal) Transmit negative output (reversed)

Table 15: Location of the Ethernet signals

The Ethernet PHY provides MII/RMII/SMII interfaces to transmit and receive data. In addition the PHY also supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet PHY also features LinkMD cable diagnostics, which allows detection of common cabling plant problems such as open and short circuits.

The physical memory area for the Fast Ethernet controller is defined in *Table 16*.

Address	Function
0x1002_B + 0x000-1FF	Control/Status Registers
0x1002_B + 0x200-3FF	MIB Block Counters

Table 16: Fast Ethernet controller memory map

In order to connect the module to an existing 10/100Base-T network some external circuitry is required. The required 49,9 Ohm +/-1% termination resistors on the analog signals (ETH_RX±, ETH_TX±) are already populated on the module. Connection to an external Ethernet magnetics should be done using very short signal traces. The TPI+/TPI- and TPO+/TPO- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

An example for the external circuitry is shown in the phyCARD's Design Guide.

If you are using the applicable Carrier Board for the phyCARD-S (part number PBA-A-01), the external circuitry mentioned above is already integrated on the board (refer to *section 17.3.4).*

Caution!
Please see the datasheet of the Ethernet PHY as well as the phyCARD's Design Guide when designing the Ethernet transformer circuitry.

9.4.2 Software Reset of the Ethernet PHY (J1)

J1 connects the reset input of the Ethernet PHY (U38) with GPIO PC30. Thereby it is possible to perform a reset of the Ethernet PHY, not only by hardware, but also by software.

The following configurations are possible:

Software reset of the Ethernet PHY	J1
Software reset disabled	**open**
Software reset possible via GPIO PC30	closed

Table 17: Software Reset of the Ethernet PHY [1]

9.4.3 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCARD-S is located on the bar code sticker attached to the module. This number is a 12-digit HEX value.

[1] Defaults are in **bold blue** text

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9.5 I²C Interface

The Inter-Integrated Circuit (I^2C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The i.MX27 contains two identical and independent I^2C modules. The interface of the first module is available on the phyCARD-Connector., whereas the second module connects to the on-board EEPROM (refer to *section 7.3*). The following table lists the I^2C port on the phyCARD-Connector:

PIN #	SIGNAL	I/O	SL	DESCRIPTION
X2A17	X_I2C_CLK	O	VCC_LOGIC	I2C Clock Output
X2B17	X_I2C_DATA	I/O	VCC_LOGIC	I2C Data

Table 18: I^2C Interface Signal Location

9.6 SPI Interface

The Serial Peripheral Interface (SPI) interface is a six-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The i.MX27 contains three SPI modules. The interface signals of the first module (CSPI1) are made available on the phyCARD-Connector. This module is Master/Slave configurable. Due to the specification of the X-Arc bus, only two of the three chips-selects are available on the phyCARD-Connector. The following table lists the SPI signals on the phyCARD-Connector:

PIN #	SIGNAL	I/O	SL	DESCRIPTION
X2A35	X_CSPI1_SS0	O	VCC_LOGIC	SPI 1 Chip select 0
X2B35	X_CSPI1_SS1	O	VCC_LOGIC	SPI 1 Chip select 1
X2A36	X_#CSPI1_RDY	O	VCC_LOGIC	SPI 1 SPI data ready in Master mode
X2A37	X_CSPI1_SCLK	O	VCC_LOGIC	SPI 1 clock
X2B36	X_CSPI1_MOSI	I/O	VCC_LOGIC	SPI 1 Master data out; slave data in
X2B37	X_CSPI1_MISO	I/O	VCC_LOGIC	SPI 1 Master data in; slave data out

Table 19: SPI Interface Signal Location

9.7 Synchronous Serial Interface (SSI)

The Synchronous Serial Interface (SSI) interface of the phyCARD-S is a full-duplex, serial port that allows to communicate with a variety of serial devices, such as standard codecs, digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I^2S) and Intel AC97 standard.

With reference to the X-Arc bus specification, the main purpose of this interface is to connect to an external codec, such as AC97. In AC97 mode the clock and the frame sync signal are synchronous for the receive and transmit sections of the i.MX27 SSI module. Thus only four signals extend from the i.MX27 Digital Audio MUX (AUDMUX) to the phyCARD-Connector (SSI1_TXDAT, SSI1_RXDAT, SSI1_CLK, SSI1_FSTXDAT). AC_INT and SSI1_RES are two additional pins assisting the functionality of this interface. AC_INT is used as input and output. As output it signals which codec is supported by the phyCARD. Use of this pin as an input enables to attach an external interrupt to port PC24. SSI1_RES is connected to port PC28 of the i.MX27allowing to perform a software reset for the device attached to the interface. Please also read the phyCARD Design-In Guide for more information about how to use the AC97 interface.

Pin #	Signal	I/O	SL	Description
X2A42	AC_INT	I/O	VCC_LOGIC	AC97 Interrupt Input
X2A43	SSI1_TXDAT	O	VCC_LOGIC	AC97 Transmit Output
X2A44	SSI1_RXDAT	I	VCC_LOGIC	AC97 Receive Input
X2B42	SSI1_CLK	I	VCC_LOGIC	AC97 Clock
X2B43	SSI1_FS	O	VCC_LOGIC	AC97 SYNC
X2B44	SSI1_RES	O	VCC_LOGIC	AC97 Reset

Table 20: SSI Interface Signal Location

10 General Purpose I/Os

The X-Arc bus provides 3 GPIO / IRQ signals. *Table 21* shows the location of the GPIO / IRQ pins on the phyCARD-Connector, as well as the corresponding ports of the i.MX27.

Pin #	Signal	I/O	SL	Description
X2A46	GPIO0_IRQ	I/O	VCC_LOGIC	GPIO0 connected to µC port PC31
X2A47	GPIO2_IRQ	I/O	VCC_LOGIC	GPIO2 connected to µC port PE5
X2B47	GPIO1_IRQ	I/O	VCC_LOGIC	GPIO1 connected to µC port PC25

Table 21: Location of GPIO and IRQ pins

As can be seen in the table above the voltage level is VCC_LOGIC, which is 2.775V. In other words VCC_LOGIC is not identical with the supply voltage of the phyCARD-S. To avoid mismatch of the different voltage levels external devices connected to these pins should be supplied by VCC_LOGIC available at X2A5 and X2B5 (refer to *section 4.4*). Alternatively an open drain circuit with a pull-up resistor attached to VCC_LOGIC can be connected to the GPIOs of the phyCARD_S.

Please refer to the chapter "GPIOs" in the phyCARD Design-In Guide for more information about how to integrate the GPIO pins in your design.

11 Debug Interface (X1)

The phyCARD-S is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends to a 2.0 mm pitch pin header at X1 on the edge of the module PCB. *Figure 9* and *Figure 10* show the position of the debug interface (JTAG connector X1) on the phyCARD-S module.

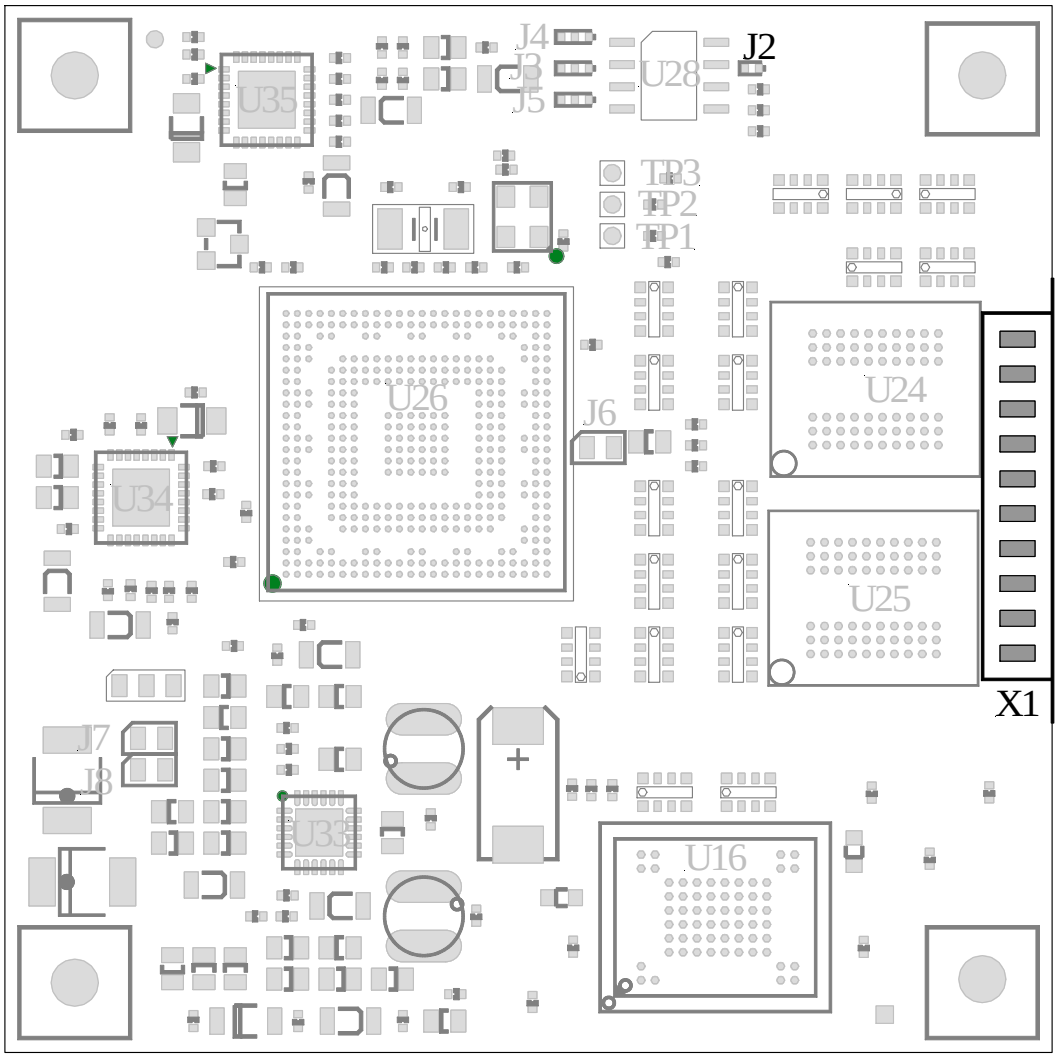

Figure 9: JTAG interface at X1 (top view)

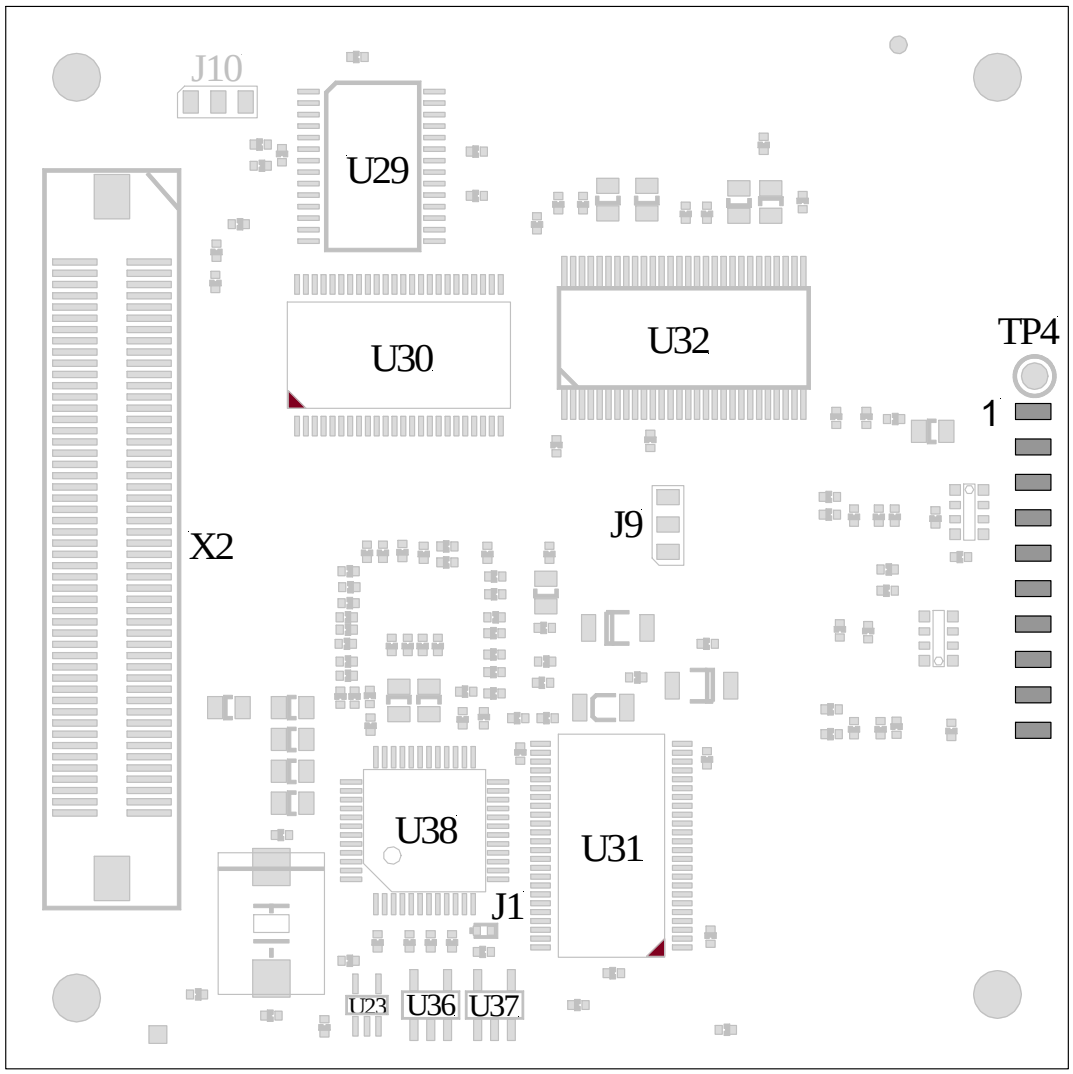

Figure 10*: JTAG interface at X1 (bottom view)*

Pin 1 of the JTAG connector X1 is on the connector side of the module. Pin 2 of the JTAG connector is on the controller side of the module.

Note:
The JTAG connector X1 only populates phyCARD-S modules with order code PCA-A-S1-D. JTAG connector X1 is not populated on phyCARD modules with order code PCA-A-S1. We recommend integration of a standard (2 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface.

See *Table 22* for details on the JTAG signal pin assignment.

Signal	Pin Row*		Signal
	A	B	
VCCLOGIC	2	1	TREF (VCCLOGIC via 100 Ohm)
GND	4	3	x_#TRST
GND	6	5	x_TDI
GND	8	7	x_TMS
GND	10	9	x_TCK
GND	12	11	x_RTCK
GND	14	13	x_TDO
GND	16	15	x_#RESET
GND	18	17	n.c.
GND	20	19	J_DBGACK (10k Ohm pulldown)

Table 22: JTAG connector X1 signal assignment

*Note: Row A is on the controller side of the module and row B is on the connector side of the module

PHYTEC offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyCARD-S to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X1 to standard Emulator connectors.

12 LVDS Display Interface

The phyCARD-S uses a DS90C383 4-Channel 24-Bit LVDS Transmitter (U32) to generate LVDS-Signals from the parallel TTL Display Interface. Thus you can connect a LVDS-Display to the phyCARD-S. The location of the applicable interface signals (TXOUT1-3+/TXOUT1-3-/TXCLK+/TXCLK-) can be found in the table below.

Pin #	Signal	I/O	SL	Description
X2A9	TXOUT0+	O	LVDS	LVDS Chanel 0 positive Output
X2A10	TXOUT0-	O	LVDS	LVDS Chanel 0 negative Output
X2A11	TXOUT2+	O	LVDS	LVDS Chanel 2 positive Output
X2A12	TXOUT2-	O	LVDS	LVDS Chanel 2 negative Output
X2A14	TXCLKOUT+	O	LVDS	LVDS Clock positive Output
X2A15	TXCLKOUT-	O	LVDS	LVDS Clock negative output
X2B9	TXOUT1+	O	LVDS	LVDS Chanel 0 positive Output
X2B10	TXOUT1-	O	LVDS	LVDS Chanel 0 negative Output
X2B11	TXOUT3+	O	LVDS	LVDS Chanel 3 positive Output
X2B12	TXOUT3-	O	LVDS	LVDS Chanel 3 negative Output

Table 23: Display Interface Signal Location

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12.1 Signal configuration (J9, J11)

J9 selects rising, or falling edge strobe for the LVDS Transmitter at U32 used for the display connectivity of the phyCARD-S.

Position	Description	Type
1+2	**rising edge strobe used for the LVDS display signals**	10k (0805)
2+3	falling edge strobe used for the LVDS display signals	

J11 selects either signal OE_ACD, or PS as data enable of the display interface

Position	Description	Type
1+2	**OE_ACD used as data enable**	0R (0805)
2+3	PS used as data enable	

Most of the displays work with the default configuration of these jumpers and changing them is usually not necessary.

12.2 LVDS Display Interface pixel mapping

The phyCARD specification defines the pixel mapping of the LVDS display interface. The pixel mapping equates to the OpenLDI respectively Intel 24.0 standard. Thus you can connect 18-bit as well as 24-bit LVDS displays to the phyCARD. *Table 24* and *Table 25* show the recommended pixel mapping of the LVDS display. For further information please see the phyCARD Design Guide.

Note:
Make sure that the LVDS display you want to use provides the same pin mapping as the phyCARD. Normally this is only important for 24-bit LVDS displays because due to the organization of the LVDS pixel mapping all common 18-bit LVDS displays should work.

18-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G0	R5	R4	R3	R2	R1	R0
A1	B1	B0	G5	G4	G3	G2	G1
A2	DE	VSYNC	HSYNC	B5	B4	B3	B2
A3	0	0	0	0	0	0	0

Table 24: Pixel mapping of 18-bit LVDS display interface

24-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G2	R7	R6	R5	R4	R3	R2
A1	B3	B2	G7	G6	G5	G4	G3
A2	DE	VSYNC	HSYNC	B7	B6	B5	B4
A3	0	B1	B0	G1	G0	R1	R0

Table 25: Pixel mapping of 24-bit LVDS display interface

13 LVDS Camera Interface

The phyCARD-S uses a DS92LV1212A 1-channel 10-Bit LVDS Random Lock Deserializer (U29) to receive LVDS-Signals from a LVDS Camera Interface. The LVDS Deserializer converts the LVDS signal to a 10-bit wide parallel data bus and separate clock which can be used as inputs for the i.MX27 Camera Sensor Interface. The 10-bit wide databus consist of 8 color information bits and 2 sync bits (HSYNC/VSYNC).

The following table shows the location of the applicable interface signals (LVDS_CAM_MCLK, LVDS_CAM_nLOCK, LVDS_CAM_RX+, LVDS_CAM_RX-) on the phyCARD-Connector.

Pin #	Signal	I/O	SL	Description
X2A16	X_CSI_MCLK	O	VCC_LOGIC	Clock Output for Camera Interface
X2B14	RXIN+	O	LVDS	LVDS Receive positive Input for Camera
X2B15	RXIN-	O	LVDS	LVDS Receive negative Input for Camera
X2B16	LOCK	O	VCC_LOGIC	Lock Output for Camera Interface

Table 26: Camera Interface Signal Location

13.1 Signal configuration (J10)

J10 selects rising, or falling edge strobe for the LVDS Deserializer at U29 used for the display connectivity of the phyCARD-S

Position	Description	Type
1+2	**rising edge strobe used for the LVDS camera signals**	10k (0805)
2+3	falling edge strobe used for the LVDS camera signals	

14 Technical Specifications

The physical dimensions of the phyCARD-S are represented in Figure 11. The module's profile is approximately ***8.5 mm*** thick, with a maximum component height of ***4.0 mm*** on the bottom (connector) side of the PCB and approximately ***3.1 mm*** on the top (microcontroller) side. The board itself is approximately ***1.4 mm*** thick.

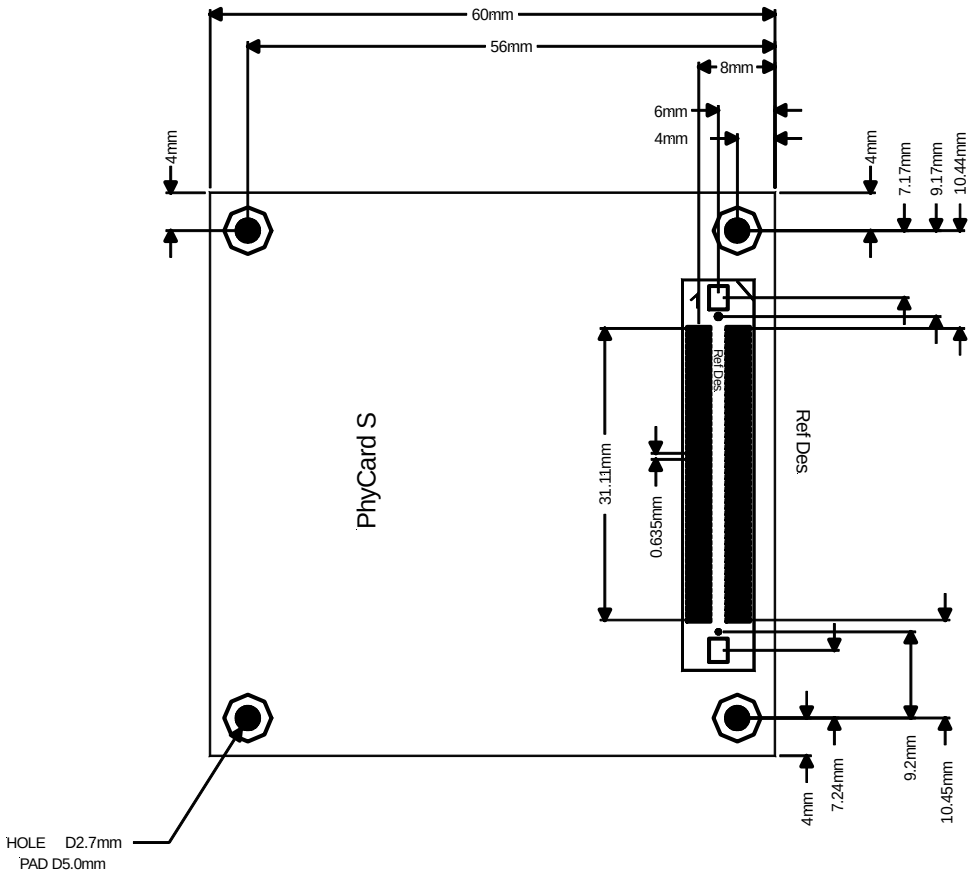

Figure 11: Physical dimensions

Note:
To facilitate the integration of the phyCRAD-S into your design, the footprint of the phyCARD-S is available upon request.

Additional specifications:

Dimensions:	60 mm x 60 mm
Weight:	approximately 16 g with all optional components mounted on the circuit board
Storage temperature:	-40°C to +125°C
Operating temperature:	0°C to +70°C (commercial) -20°C to +85°C (industrial)
Humidity:	95 % r.F. not condensed
Operating voltage:	VCC 3.3V
Power consumption: VCC 3.3 V/200mA typical	Max. 1.0 watts Conditions: **VCC = 3.3 V, VBAT = 0 V**, 32MB LP-DDR-RAM, 64MB NAND Flash, Ethernet, 400 MHz CPU frequency at 20°C

These specifications describe the standard configuration of the phyCARD-S as of the printing of this manual.

Connectors on the phyCARD:

Manufacturer	Molex
Number of pins per contact rows	100 (2 rows of 50 pins each)
Molex part number (lead free)	52885-1074 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCARD—i.MX27. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (2,5 mm) on the bottom side of the phyCORE must be subtracted.

Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	100 (2 rows of 50 pins each)
Molex part number (lead free)	55091-1075/1074 (header)

Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	100 (2 rows of 50 pins each)
Molex part number (lead free)	53553-1079 (header)

Please refer to the corresponding data sheets and mechanical specifications provided by Molex (*www.molex.com*).

15 Component Placement Diagram

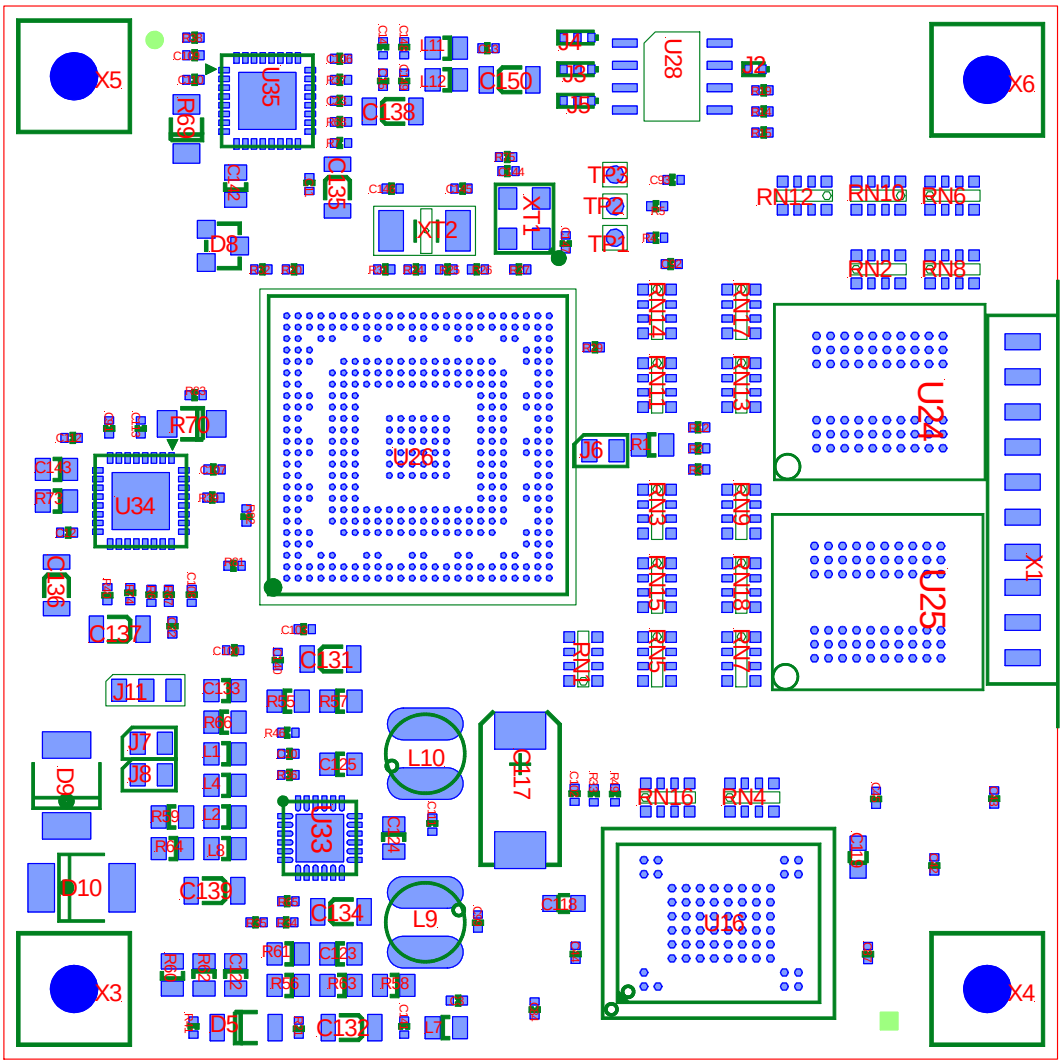

Figure 12: phyCARD-S component placement (top view)

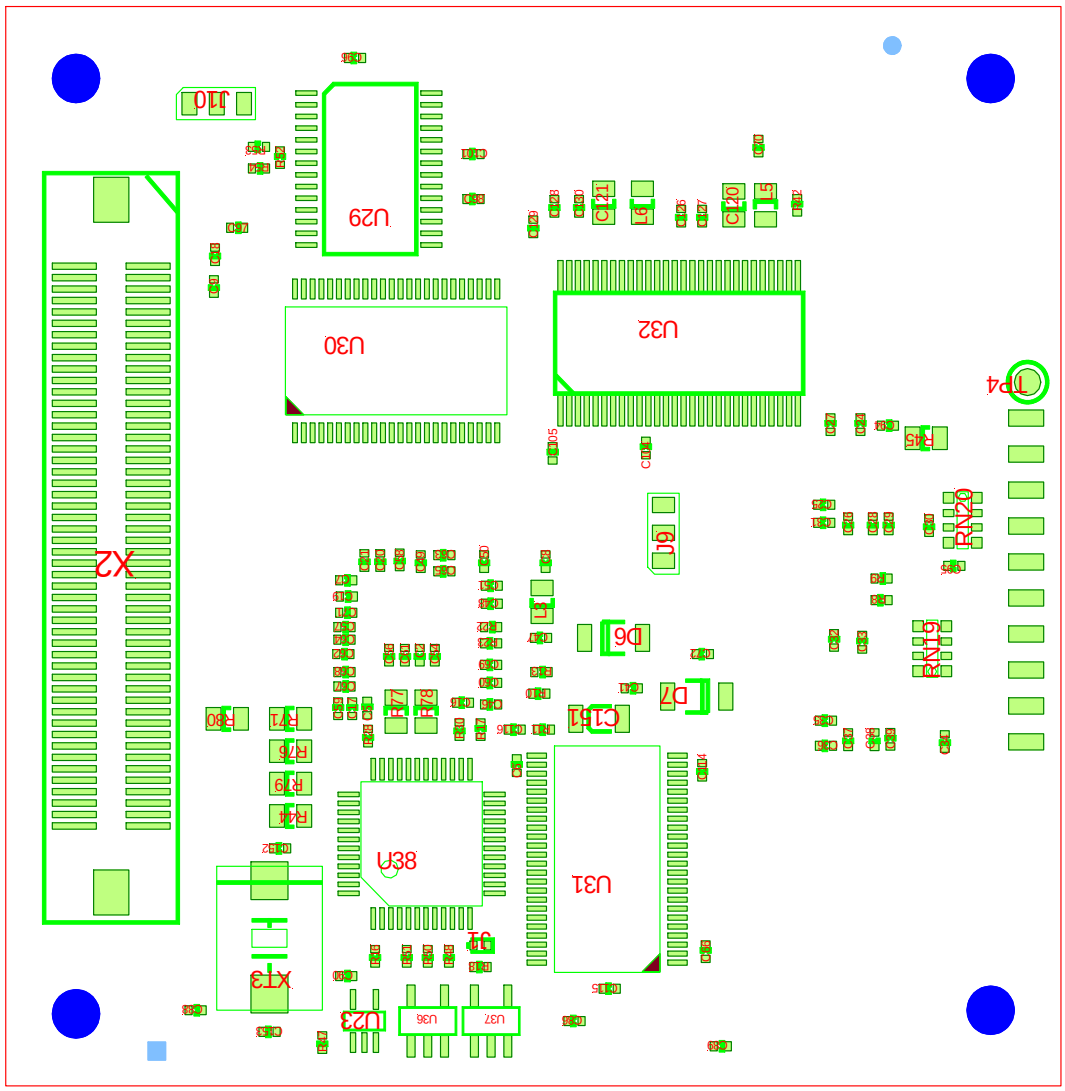

Figure 13: phyCARD-S component placement (bottom view)

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16 Hints for Handling the phyCARD-S

- **Modifications on the phyCARD Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCARD into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCARD module. For best results we recommend using a carrier board design with a full GND layer. It is important to make sure that the GND pins that have neighboring signals which are used in the application circuitry are connected. Just for the power supply of the module at least 8 GND pins that are located right next to the VCC pins must be connected

Note!
Please refer to the phyCARD Design-In Guide (LAN-051) for additional information, layout recommendations and example circuitry.

17 The phyCARD-S on the phyBase

PHYTEC phyBASE Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. phyBASE Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

The phyBASE supports the following features for the phyCARD-S modules:

- Power supply circuits to supply the modules and the peripheral devices
- Support of different power modes of appropriate phyCARDs
- Full featured 4 line RS-232 transceiver supporting data rates of up to 120kbps, hardware handshake and RS-232 connector
- Six USB-Host interfaces
- USB-OTG interface
- 10/100 Mbps Ethernet interface
- Complete Audio and Touchscreen interface
- LVDS display interface with separate connectors for data lines and display / backlight supply voltage
- Circuitry to allow dimming of a backlight
- LVDS camera interface with I^2C for camera control
- Security Digital Card / Multi Media Card Interface
- Two expansion connectors for customer prototyping purposes featuring one USB, one I^2C and on SPI interface, as well as on GPIO/IRQ at either connector
- DIP-Switch to configure various interface options
- Jumper to configure the boot options for the phyCARD-S module mounted
- RTC with battery supply/backup

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17.1 Concept of the phyBASE Board

The phyBASE Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCARD Single Board Computer module. The Carrier Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation. The Carrier Board is compatible with all phyCARDs.

This modular development platform concept is depicted in *Figure 14* below and includes the following components:

- the **phyCARD-S Module** populated with the i.MX27 processor and all applicable SBC circuitry such as DDR SDRAM, Flash, PHYs, and transceivers to name a few.

- the **phyBASE** which offers all essential components and connectors for start-up including: a power socket enabling connection to an **external power adapter**, interface connectors such as **DB-9, USB and Ethernet** allowing for use of the SBC's interfaces with standard cable.

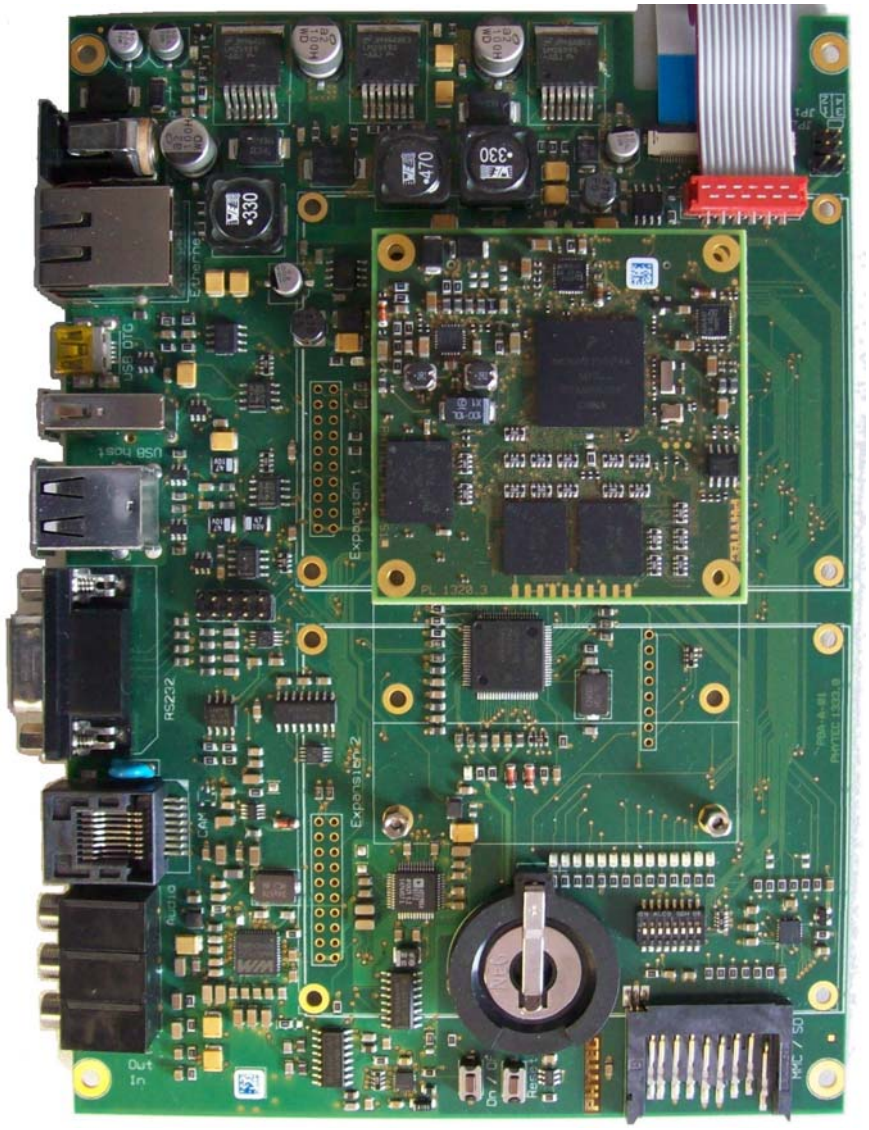

Figure 14: phyBASE (phyCARD-S Carrier Board)

The following sections contain specific information relevant to the operation of the phyCARD-S mounted on the phyBASE Carrier Board.

Note:
Only features of the phyBASE which are supported by the phyCARD-S are described. Jumper settings and configurations which are not suitable for the phyCARD-S are not described in the following chapters.

17.2 Overview of the phyBASE Peripherals

The phyBASE is depicted in *Figure 15* and includes the following components and peripherals listed in *Table 27*, *Table 28*, *Table 29* and *Table 30*. For a more detailed description of each peripheral refer to the appropriate chapter listed in the applicable table. *Figure 15* highlights the location of each peripheral for easy identification.

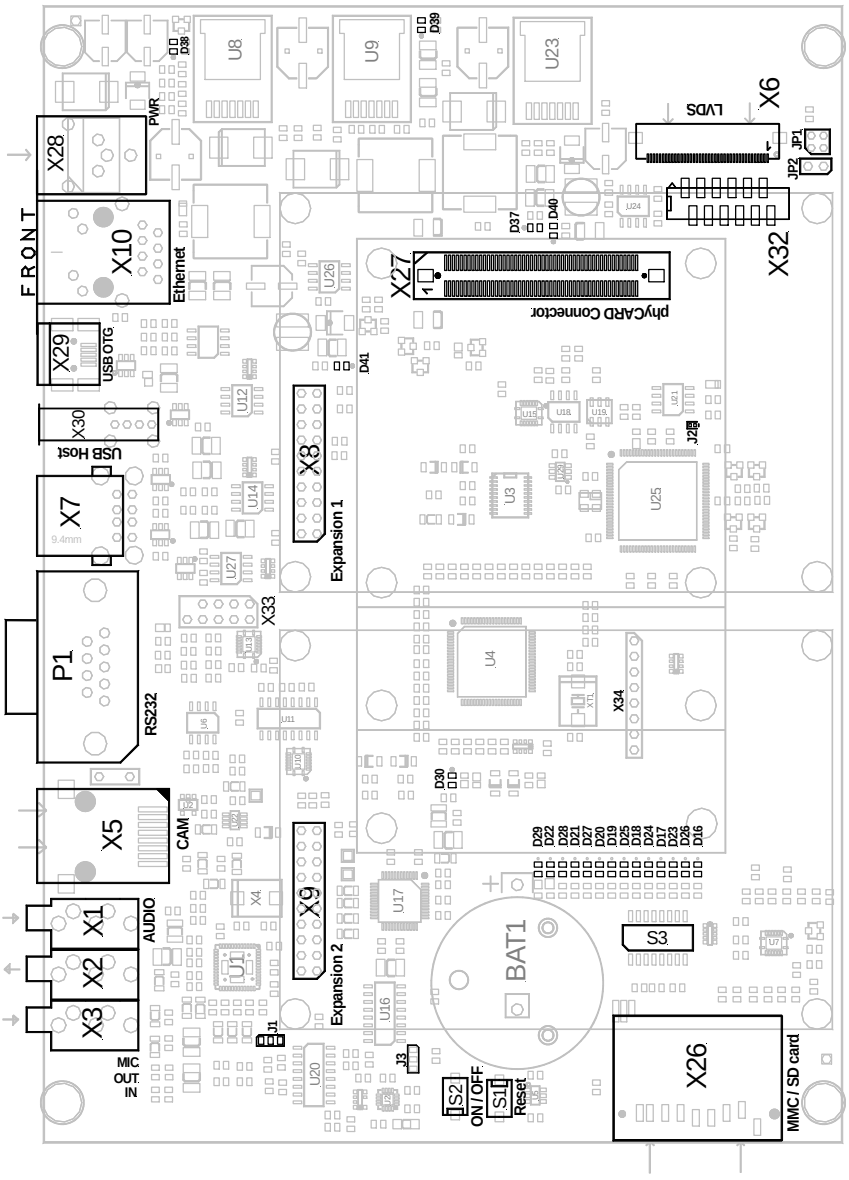

Figure 15*: phyBASE* Overview of Connectors, LEDs and Buttons

17.2.1 Connectors and Pin Header

Table 27 lists all available connectors on the phyBASE. *Figure 15* highlights the location of each connector for easy identification.

Reference Designator	Description	See Section
X1	Stereo Microphone input connector	*17.3.9*
X2	Stereo Line Out connector	*17.3.9*
X3	Stereo Line In connector	*17.3.9*
X5	Camera Interface, RJ45	*17.3.8*
X6	Display data connector	*17.3.7.1*
X7	Dual USB Host connector	*17.3.5*
X8A	Expansion connector 0	*17.3.13*
X9A	Expansion connector 1	*17.3.13*
X10	Ethernet connector, RJ45 with speed and link led	*17.3.4*
X26	Security Digital/MultiMedia Card slot	*17.3.14*
X27	phyCARD-Connector for mounting the phyCARD-S	*17.3.1*
X28	Wall adapter input power jack to supply main board power (+9 - +36 V)	*17.3.2*
X29	USB On-The-Go connector	*17.3.6*
X30	USB Host connector	*17.3.5*
X32	Display / Backlight supply voltage connector	*17.3.7.2*
X33	USB Host connector	*17.3.5*
X34	CPLD JTAG connector	**for internal use only**
P1	Serial Interface, DB-9F	*17.3.3*

Table 27: phyBASE Connectors and Pin Headers

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Note:
The signal levels of the I^2C and SPI interface are shifted from VCC_LOGIC (2.75V) at the phyCARD Connector to VCC3V3 (3.3 V) by level shifters on the phyCARD Carrier Board.
Ensure that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user‘s responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

17.2.2 Switches

The phyBASE is populated with some switches which are essential for the operation of the phyCARD-S module on the Carrier Board. *Figure 15* shows the location of the switches and push buttons.

Button	Description	See Section
S1	System Reset Button – system reset signal generation	*17.3.16*
S2	Power Button – powering on and off main supply voltages of the Carrier Board	*17.3.2*

Table 28: phyBASE push buttons descriptions

S1 Issues a **system reset** signal. Pressing this button will toggle the nRESET_IN pin of the phyCARD microcontroller LOW, causing the controller to reset.

S2 Issues a **power on/off** event. Pressing this button less than 2 seconds will toggle the nPWR_KEY pin of the phyBASE CPLD LOW, causing the CPLD to turn on the supply voltages, pressing this button for more than 2 seconds causing the CPLD to turn off the supply voltages.

Additionally a DIP-Switch is available at S3. The following table gives an overview of the functions of the DIP-switch.

Note:
The following table describes only settings suitable for the phyCARD-S. Other settings must not be used with the phyCARD-S.

Button	Setting	Description	See Section
S3_1/ S3_2	**0/0** 0/1 1/0	Switches 1 and 2 of DIP-Switch S3 select which device process the audio and touch panel signals. **Wolfson audio/touch contrl. (U1) selected for touch and audio** Wolfson audio/touch contrl. (U1) selected for audio, dedicated touch contrl. (U28) for touch Analog Devices audio contrl. (U17) selected for audio, dedicated touch contrl. (U28) for touch	*17.3.9*
S3_3/ S3_4	**0/0**	Switches 3 and 4 of DIP-Switch S3 configure the I^2C address for the communication between CPLD and phyCARD. **CPLD Address 0x80**	
S3_5	**0**1	Switch 5 of DIP-Switch S3 selects the interface used for the communication between CPLD and phyCARD. **I2C communication selected**	
S3_6	**0**	Switch 6 of DIP-Switch S3 turns the SPI Multiplexer on, or off **SPI multiplexer off**	

S3_7/ S3_8	**0/0** 0/1 1/x	Switches 7 and 8 of DIP-Switch S3 map the two slave select signals of the SPI interface and the two GPIO_IRQ signals (GIO0_IRQ, GPIO1_IRQ) to two of the three available connectors. **SS0/GPIO0 -> expansion 0 (X8A),** **SS1/GPIO1 -> expansion 1 (X9A)** SS0/GPIO0 -> expansion 0 (X8A), SS1/GPIO1 -> display data connector (X6) SS0/GPIO0 -> expansion 1 (X9A), SS1/GPIO1 -> display data connector (X6)	*17.3.7.1* *17.3.11* *17.3.12* *17.3.13*

Table 29: phyBASE DIP-Switch S3 descriptions[1]

[1] Default settings are in **bold blue** text

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17.2.3LEDs

The phyBASE is populated with numerous LEDs to indicate the status of the various USB-Host interfaces, as well as the different supply voltages. *Figure 15* shows the location of the LEDs.

LED	Color	Description	See Section
D16	yellow	USB1 amber led	
D17	yellow	USB2 amber led	
D18	yellow	USB3 amber led	
D19	yellow	USB4 amber led	
D20	yellow	USB5 amber led	
D21	yellow	USB6 amber led	
D22	yellow	USB7 amber led	
D23	green	USB1 green led	*17.3.5*
D24	green	USB2 green led	
D25	green	USB3 green led	
D26	green	USB4 green led	
D27	green	USB5 green led	
D28	green	USB6 green led	
D29	green	USB7 green led	
D30	red	USB HUB global led	
D37	green	5V supply voltage for peripherals on the phyBASE	
D38	green	supply voltage of the phyCARD	
D39	green	3V3 supply voltage for peripherals on the phyBASE	*17.3.2*
D40	green	3V3 standby voltage of the phyBASE	
D41	green	standby voltage of the phyCARD	

Table 30: phyBASE LEDs descriptions

Note:
Detailed descriptions of the assembled connectors, jumpers and switches can be found in the following chapters.

17.2.4 Jumpers

The phyCARD Carrier Board comes pre-configured with 2 removable jumpers (JP) and 3 solder jumpers (J). The jumpers allow the user flexibility of configuring a limited number of features for development constraint purposes. *Table 31* below lists the 5 jumpers, their default positions, and their functions in each position. *Figure 16* depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board. Note that pin 1 is always marked by a square footprint in the jumper location diagrams that follow.

Figure 17 provides a detailed view of the phyBase jumpers and their default settings.

Before making connections to peripheral connectors it is advisable to consult the applicable section in this manual for setting the associated jumpers.

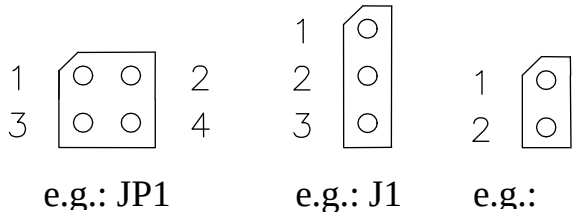

Figure 16: Typical jumper numbering scheme

Table 31 provides a comprehensive list of all Carrier Board jumpers. The table only provides a concise summary of jumper descriptions. For a detailed description of each jumper see the applicable chapter listing in the right hand column of the table.

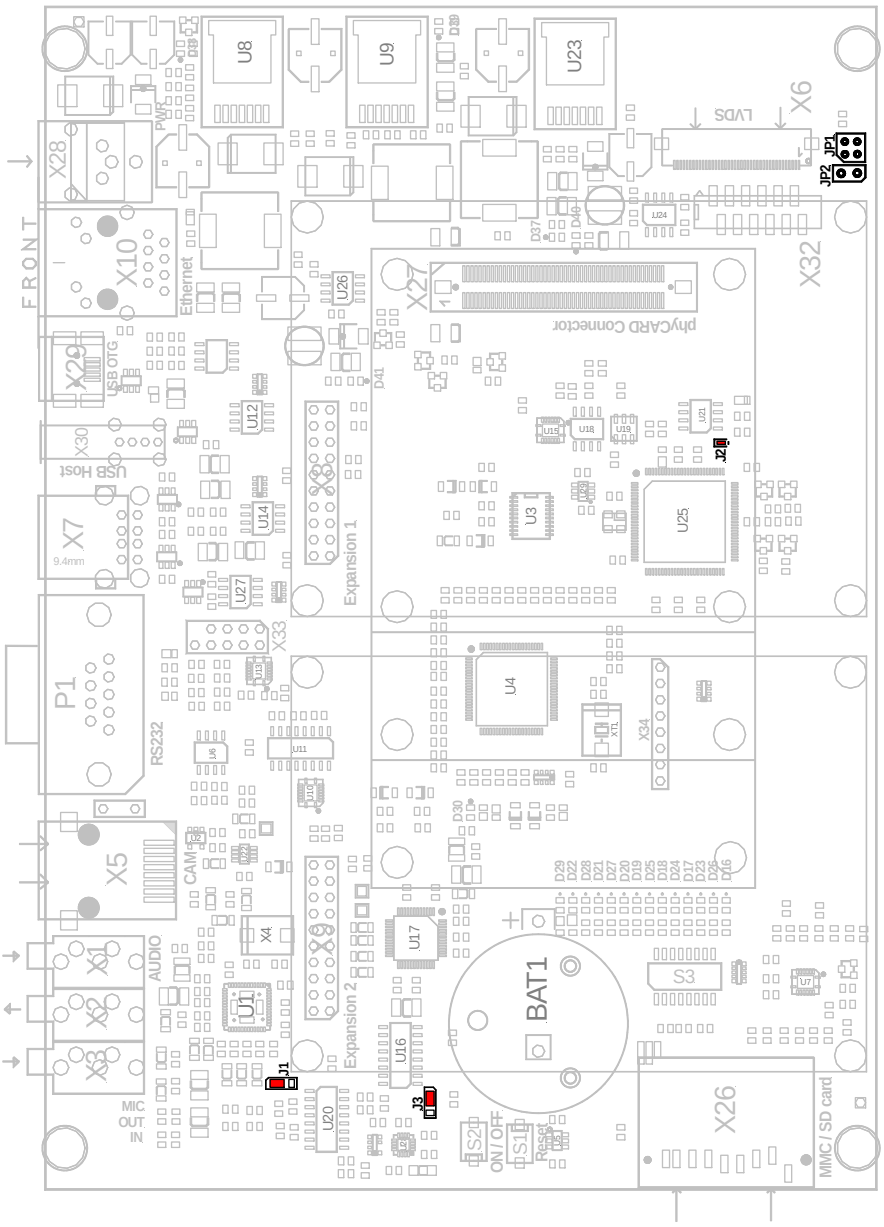

Figure 17: phyBASE jumper locations

The following conventions were used in the Jumper column of the jumper table (*Table 31)*

- J = solder jumper
- JP = removable jumper

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Jumper	Setting	Description	See Section
JP1	**open**	Jumper JP1 selects the boot device of the phyCARD-S **FLASH enabled as Boot device**	*17.3.3*
	1+2	internal ROM of the i.MX27 enabled as Boot device and thus starting the bootstrap program	
		other settings must not be used with the phyCARD-S	
JP2	**open**	Jumper JP2 connects the input voltage to connector X32 as supply voltage for a backlight. **VCC12V Backlight disabled**	*17.3.7.2*
	closed	**VCC12V Backlight connected to power supply only 12V DC power supplies allowed**	
J1	**1+2**	Jumper J1 selects the function of the AC97 interrupt **Pendown signal of the Audio/Touch controller at U1 is connected to AC97 interrupt**	*17.3.7.3*
	2+3	GPIO2_IRQ output of the Audio/Touch controller at U1 connected to AC97 interrupt	
J2	**closed**	Jumper J2 configures the I^2C address of the LED dimmer at U21 **I^2C device address of LED dimmer set to 0xC0**	*17.3.7.2* *17.3.10*
	open	I^2C device address of LED dimmer set to 0xC2	

J3		Jumper J3 configures the I^2C address of the touch screen controller at U28	*17.3.7.3* *17.3.10*
	1+2	**I^2C device address set to 0x88**	
	2+3	I^2C device address set to 0x82	

Table 31: phyBASE jumper descriptions[1]

[1] Default settings are in **bold blue** text

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17.3 Functional Components on the phyBASE Board

This section describes the functional components of the phyBASE Carrier Board supporting the phyCARD-S. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

17.3.1 phyCARD-S SBC Connectivity (X27)

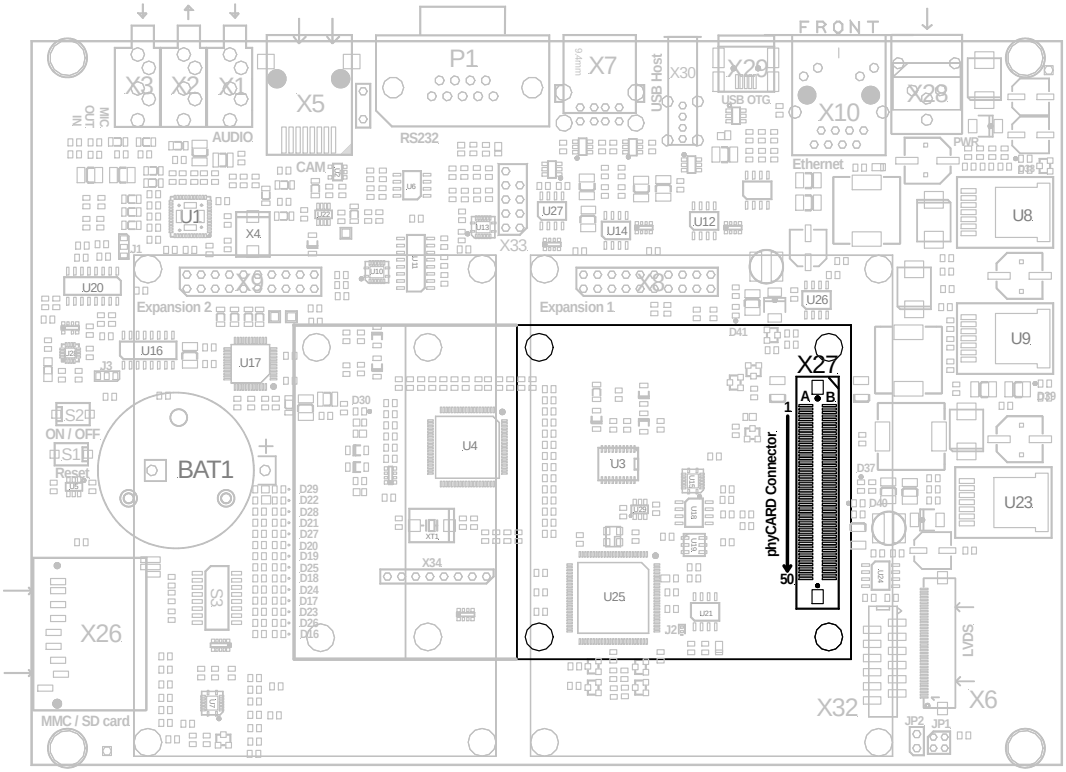


Figure 18: phyCARD-S SBC Connectivity to the Carrier Board

Connector X27 on the Carrier Board provides the phyCARD System on Module connectivity. The connector is keyed for proper insertion of the SBC. *Figure 18* above shows the location of connector X27, along with the pin numbering scheme as described in *section 1.*

17.3.2 Power Supply (X28)

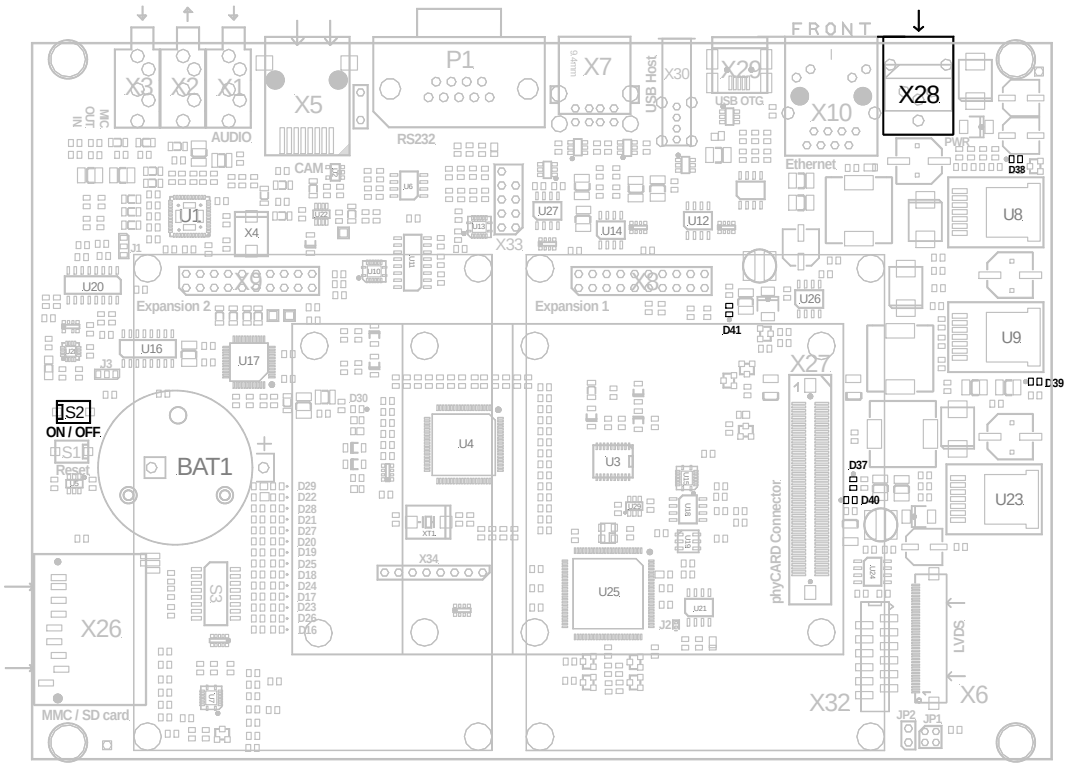


Figure 19: Power adapter

Caution:
Do not use a laboratory adapter to supply power to the Carrier Board! Power spikes during power-on could destroy the phyCARD-module mounted on the Carrier Board! Do not change modules or jumper settings while the Carrier Board is supplied with power!

Permissible input voltage at X28: +9 - +36 V DC unregulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCARD mounted on the Carrier Board as well as whether an optional expansion board is connected to the Carrier Board. An adapter with a minimum supply of 2.0 A is recommended.

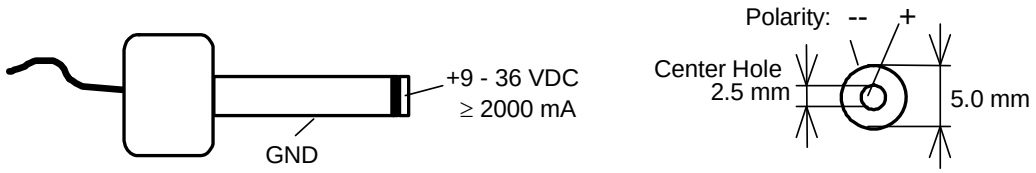


Figure 20: Connecting the Supply Voltage at X28

No jumper configuration is required in order to supply power to the phyCARD module!

The phyBASE is assembled with a few power LEDs whose functions are described in the following table:

LEDs	Color	Description
D37	green	VCC5V led
D38	green	VCC_PHYCARD led
D39	green	VCC3V3 led
D40	green	VCC3V3STBY led
D41	green	VSTBY led

Table 32: LEDs assembled on the Carrier Board

Note:
For powering up the phyCARD the following actions have to be done:

1. Plug in the power supply connector
   » All power LEDs should light up and the phyCARD puts serial output to serial line 0 at P1.
2. For powering down the phyCARD-S button S2 should be pressed for a minimum time of 2000ms.
3. Press button S2 for a maximum time of 1000ms seconds.
   » All power LEDs should light up and the phyCARD puts serial output to serial line 0 at P1.

Three different power states are possible RUN, OFF and SUSPEND.

- During RUN all supply voltages except VSTBY are on. This means that the phyCARD-S is supplied by VCC_PHYCARD.
- In OFF state all supply voltages are turned off. Only the standby voltage (VCC3V3STBY) of the phyBASE itself is still available to supply the PLD, the RTC and to provide a high-level voltage for the Reset and Power switch.
- In SUSPEND mode only the standby voltage VSTBY for the phyCARD-S and the standby voltage (VCC3V3STBY) of the phyBASE itself are generated. This means the phyCARD-S is supplied only by VSTBY.

The RUN and OFF state can be entered using the power button S2 as described in the gray box above. It is also possible to enter OFF state with the help of the phyCARD's X_#PWR_OFF signal (PC17 of the i.MX27). To enter OFF state signal X_#PWR_OFF must be active (low).

SUSPEND state can be entered using signal X_#SUSP_RAM at pin X2A26B of the phyCARD Connector (PC16 of the i.MX27). X_#SUSP_RAM must be active (low) for at least 500ms.

17.3.3 RS-232 Connectivity (P1)

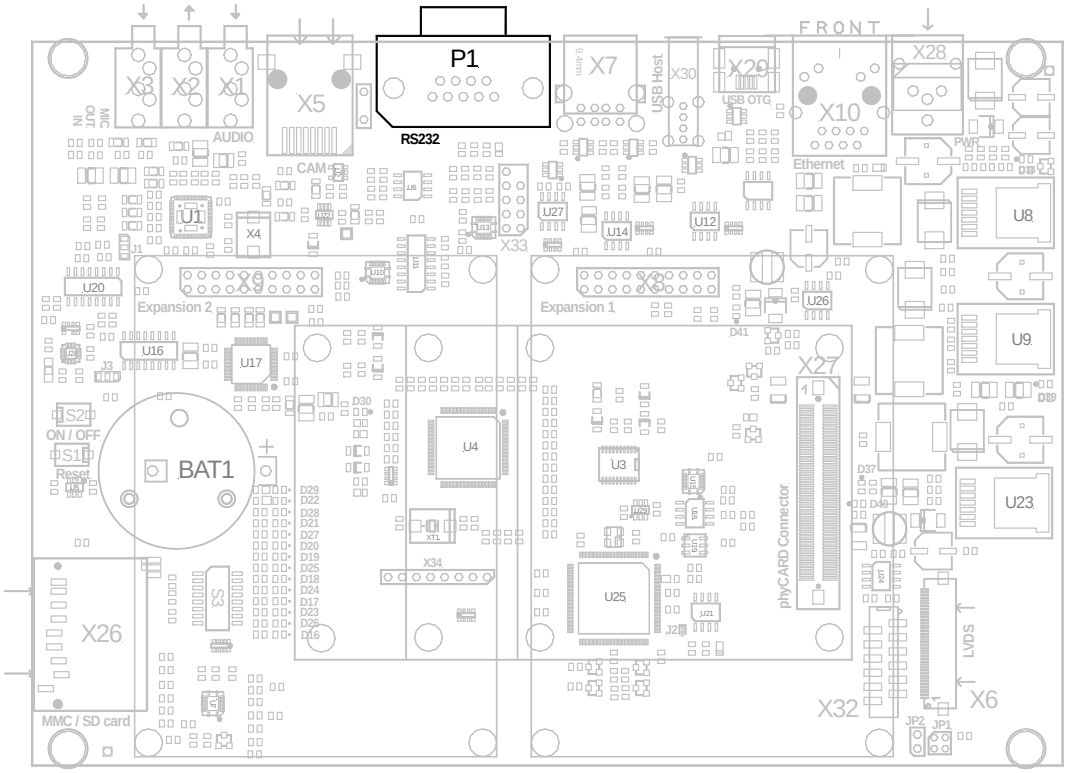
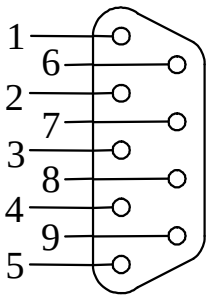


Figure 21*: UART1 connection interface at connector P1*

Connector P1 is a DB9 sub-connector and provides a connection interface to UART1 of the i.MX27. The TTL level signals from the phyCARD-S are converted to RS-232 level signals. UART1 provides only two handshake signals: RTS and CTS. *Figure 22* below shows the signal mapping of the RS-232 level signals to connector P1.



Pin 2:	TxD-RS232
Pin 7:	RTS-RS232
Pin 3:	RxD-RS232
Pin 8:	CTS-RS232
Pin 5:	GND

Figure 22: UART1 connector P1 signal description

The RS-232 interface is hard-wired and no jumpers must be configured for proper operation.

17.3.4 Ethernet Connectivity (X10)

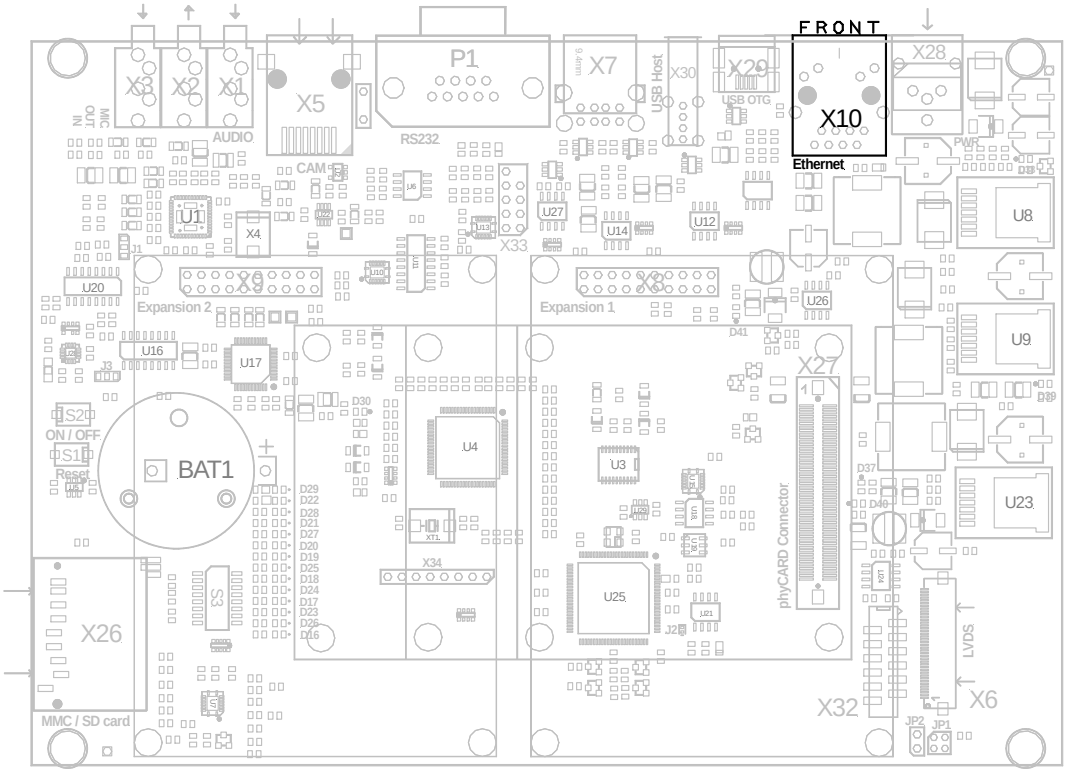


Figure 23*: Ethernet interface at connector X10*

The Ethernet interface of the phyCARD is accessible at an RJ45 connector (X10) on the Carrier Board. Due to its characteristics this interface is hard-wired and can not be configured via jumpers. The LEDs for LINK and SPEED indication are integrated in the connector.

17.3.5 USB Host Connectivity (X7, X8, X9, X30, X33)

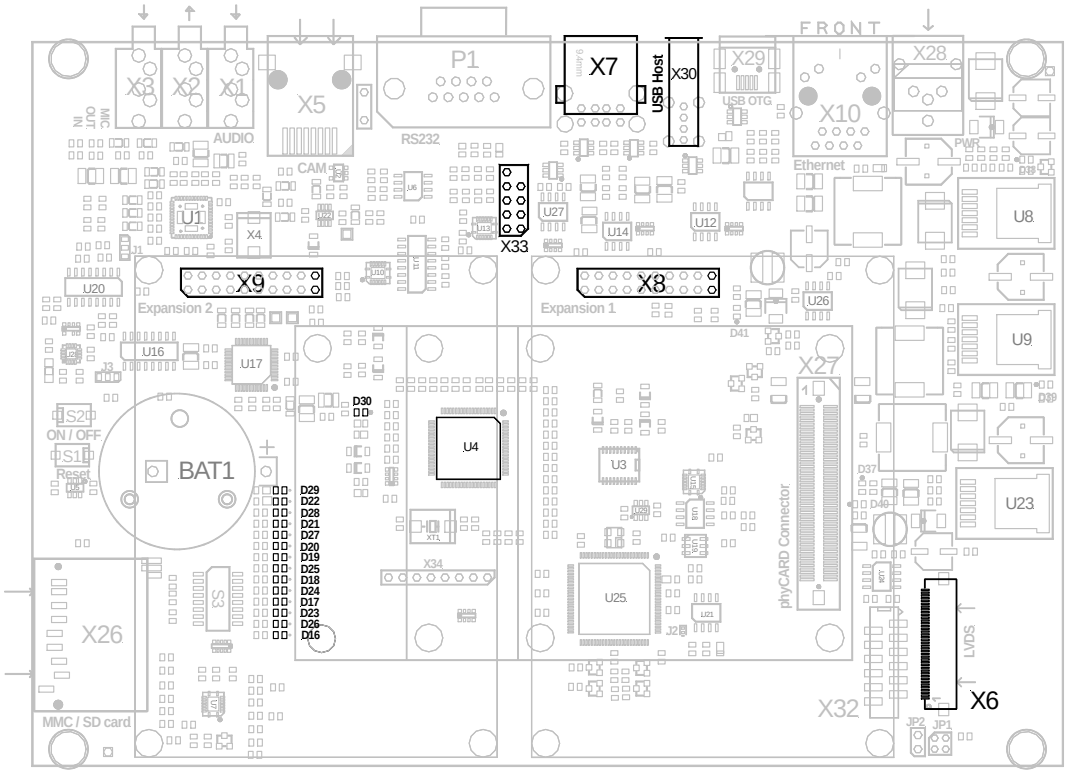


Figure 24: USB host interface at connector X7, X30, X33

The USB host interface of the phyCARD is accessible via the USB hub controller U4 on the Carrier Board. The controller supports control of input USB devices such keyboard, mouse or USB key. The USB hub has 7 downstream facing ports. Three ports extend to standard USB connectors at X7 (dual USB A) and X30 (USB A). A fourth port connects to 9 pin header row X33. These interfaces are compliant with USB revision 2.0. The remaining ports are accessible at the display data connector X6 and the expansion connectors X8A and X9A. These three interfaces provide only the data lines D+ and D-. They do not feature a supply line Vbus.

LEDs D16 to D30 signal use of the USB host interfaces. *Table 30* shows the assignment of the LEDs to the different USB ports.

Table 33 shows the distribution of the seven downstream facing ports to the different connectors, whereas *Table 34* shows the Pin-out of USB host connector X33.

USB hub port #	Connector	Connector Type
USB1	X30	USB A
USB2	X6	40 pin FCC (pins 16 and 17)
USB3	X8	20 pin header row (pins 19 and 20)
USB4	X9	20 pin header row (pins 19 and 20)
USB5	X33	9 pin header row (see table below)
USB6	X7A (bottom)	USB A
USB7	X7B (top)	USB A

Table 33: Distribution of the USB hub's (U4) ports

Pin number	Signal name	Description
1	USB5_VBUS	USB5 Power Supply
3	USB5_D-	USB5 Data -
5	USB5_D+	USB5 Data +
7	GND	Ground
2,4,6,8,10	NC	Not connected

Table 34: Universal USB pin header X33 signal description

17.3.6 USB OTG Connectivity (X29)

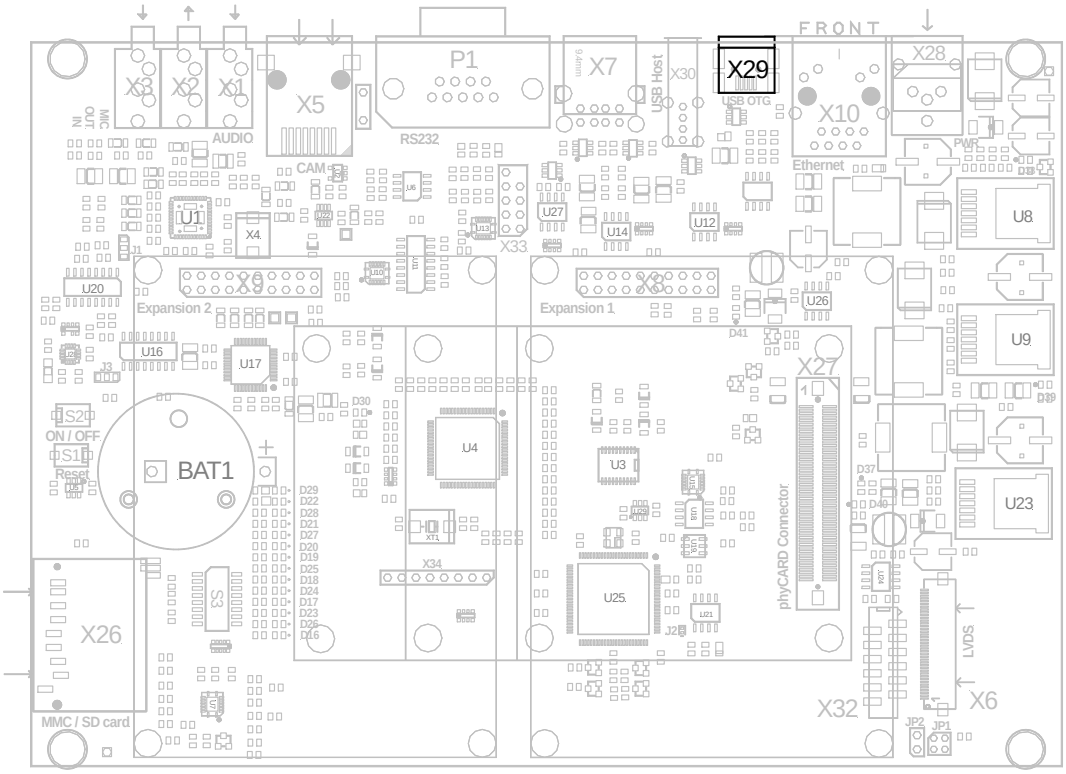


Figure 25: USB OTG interface at connector X29

The USB OTG interface of the phyCARD is accessible at connector X29 (USB Mini AB) on the Carrier Board. This interface is compliant with USB revision 2.0.

No jumper settings are necessary for using the USB OTG port.

The phyCARD supports the On-The-Go feature. The Universal Serial Bus On-The-Go is a device capable to initiate the session, control the connection and exchange Host/Peripheral roles between each other.

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17.3.7 Display / Touch Connectivity (X6, X32)

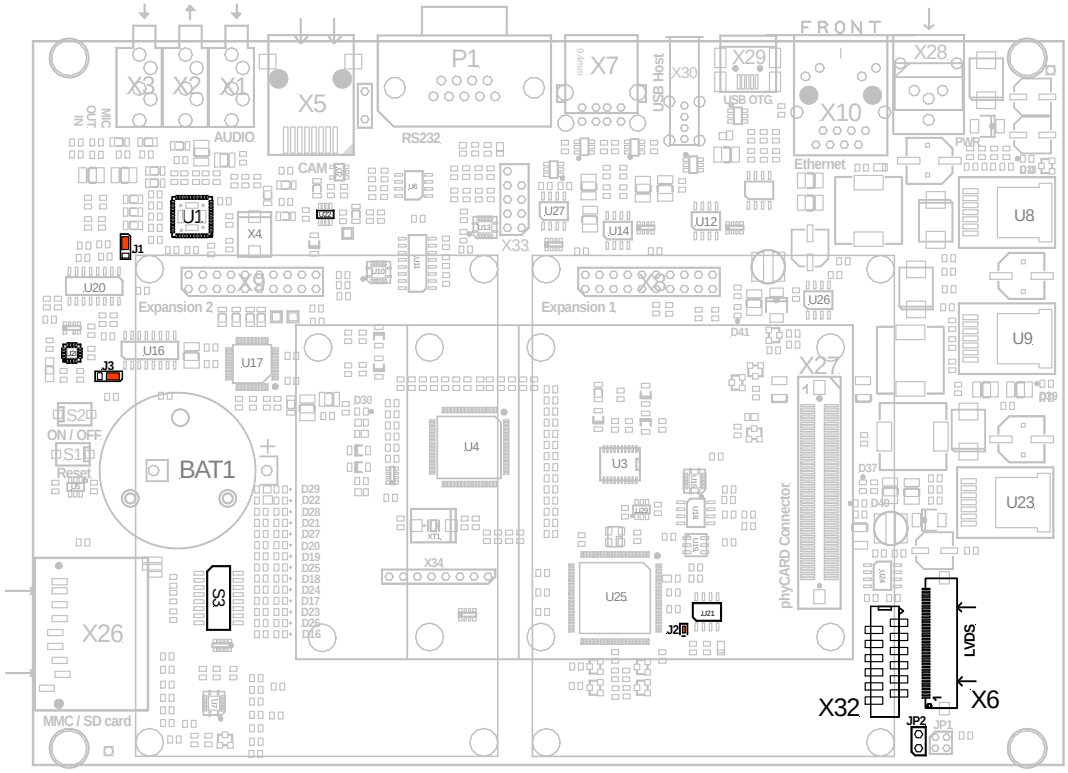

Figure 26*: Universal LVDS interface at connector X6*

The various performance classes of the phyCARD family allow to attach a large number of different displays varying in resolution, signal level, type of the backlight, Pin-out, etc. In order not to limit the range of displays connectable to the phyCARD, the phyBASE has no special display connector suitable only for a small number of displays. The new concept intends the use of an adapter board (e.g. phyBASE LCD interface LCD-014) to attach a special display, or display family to the phyCARD. Two universal connectors provide the connectivity for the display adapter. They allow easy adaption also to any customer display. The display data connector at X6 combines various interface signals like LVDS, USB, I^2C, etc. required to hook up a display. The display power connector at X32 provides all supply voltages needed to supply the display and a backlight.

17.3.7.1 Display Data Connector (X6)

The display data connector at X6 (40 pin FCC connector 0,5mm pitch) combines various interface signals.

Pin number	Signal name	Description
1	SPI1_SCLK	SPI 1 clock
2	SPI_MISO	SPI 1 Master data in; slave data out
3	SPI1_MOSI	SPI 1 Master data out; slave data in
4	SP1I_SS_DISP	SPI 1 Chip select display
5	DISP_IRQ	Display interrupt input
6	VCC3V3	Power supply display
7	I2C_SCL	I2C Clock Signal
8	I2C_SDA	I2C Data Signal
9	GND	Ground
10	LS_BRIGHT	PWM brightness Output
11	VCC3V3	Power Supply Display
12	/PWR_KEY	Power on/off Button
13	/DISP_ENA	Display enable signal
14	PHYWIRE	Hardware Introspection Interface **for internal use only**
15	GND	Ground
16	USB2_D+	USB2 data +[8]
17	USB2_D-	USB2 data -[1]
18	GND	Ground
19	TXOUT0-	LVDS data channel 0 negative output
20	TXOUT0+	LVDS data channel 0 positive output
21	GND	Ground
22	TXOUT1-	LVDS data channel 1 negative output
23	TXOUT1+	LVDS data channel 1 positive output

[8]: LEDs D17 and D24 signal use of the USB interface

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24	GND	Ground
25	TXOUT2-	LVDS data channel 2 negative output
26	TXOUT2+	LVDS data channel 2 positive output
27	GND	Ground
28	TXOUT3-	LVDS data channel 3 negative output
29	TXOUT3+	LVDS data channel 3 positive output
30	GND	Ground
31	TXCLKOUT-	LVDS clock channel negativ output
32	TXCLKOUT+	LVDS clock channel positive output
33	GND	Ground
34	TP_X+	Touch
35	TP_X-	Touch
36	TP_Y+	Touch
37	TP_Y-	Touch
38	TP_WP	Touch
39	GND	Ground
40	LS_ANA	Light sensor Analog Input

Table 35: Display data connector signal description

The X-Arc bus signals for the SPI interface and the display interrupt input are shared with the corresponding signals on the expansion connectors X8A and X9A. Because of that they have to be mapped to the display data connector by configuring switches 7 and 8 of DIP-Switch S3. The table below shows the required settings.

Button	Setting	Description
S3_7/ S3_8	**0/0**	**SS0/GPIO0[9] -> expansion 0 (X8A),** **SS1/GPIO1[1] -> expansion 1 (X9A)**
	0/1	SS0/GPIO0[1] -> expansion 0 (X8A), SS1/GPIO1[1] -> display data connector (X6)
	1/x	SS0/GPIO0[1] -> expansion 1 (X9A), SS1/GPIO1[1] -> display data connector (X6)

[9]: GPIO0 ≙ PC31 and GPIO1 ≙ PC25 of the i.MX27

Table 36: SPI and GPIO connector selection

The default setting does not connect the SPI interface and the GPIO of the X-Arc bus to the display data connector.

The Light sensor Analog Input at pin 40 extends to an A/D converter which is connected to the I^2C bus at address 0xC8 (write) and 0XC9 (read).

17.3.7.2 Display Power Connector (X32)

The display power connector X32 (AMP microMatch 8-188275-2) provides all supply voltages needed to supply the display and a backlight.

Pin number	Signal name	Description
1	GND	Ground
2	VCC3V3	3,3V power supply display
3	GND	Ground
4	VCC5V	5V power supply display
5	GND	Ground
6	VCC5V	5V power supply display
7	GND	Ground
8	VCC5V	5V power supply display
9	GND	Ground
10	LS_BRIGHT	PWM brightness output
11	VCC12V_BL	12V Backlight power supply
12	VCC12V_BL	12V Backlight power supply

Table 37: LVDS power connector X32 signal description

The PWM signal at pin 10 can be used to control the brightness of a display's backlight. It is generated by an LED dimmer. The LED dimmer is connected to the I^2C bus at address[10] 0xC0 (write) and 0xC1 (read).

To make VCC12V_BL available at X32 jumper JP2 must be closed.

Caution:
There is no protective circuitry for the backlight. Close jumper JP2 only if a 12 V power supply is connected to X28 as primary supply for the phyBASE.

17.3.7.3 Touch Screen Connectivity

As many smaller applications need a touch screen as user interface, provisions are made to connect 4- or 5- wire resistive touch screens to the display data connector X6 (pins 34 - 38, refer to *Table 35*). Two touch screen controllers are available on the phyCARD Carrier Board. The Wolfson WM9712L audio/touch codec at U1 allows connecting 4- and 5-wire touch panels, whereas the STMPE811 touch panel controller at U28 is suitable for 4-wire touch panels only. Switches 1 and 2 of DIP-Switch S3 select which controller is used to process the touch panel signals. The different configurations are shown in *Table 38*.

[10]: Default address. Jumper J2 allows to select a 0xC2 (write) and 0xC3 (read) alternatively (refer to *Table 31*).

Button	Setting	Description
S3_1/ S3_2	**0/0**	Switches 1 and 2 of DIP-Switch S3 select which device process the audio and touch panel signals. **Wolfson audio/touch contrl. (U1) selected for touch and audio**
	0/1	Wolfson audio/touch contrl. (U1) selected for audio, dedicated touch contrl. (U28) for touch
	1/0	Analog Devices audio contrl. (U17) selected for audio, dedicated touch contrl. (U28) for touch

Table 38: Selection of the touch screen controller

If the Wolfson WM9712L audio/touch codec is chosen, the touch screen data is available at the AC97 interface. An interrupt or the pendown signal of the WM9712L , selected by jumper J1 (refer to *section 17.2.4*), is connected to the AC97 interrupt pin (HAD_SEL/AC_INT, pin X2A42). The default configuration selects the pendown signal to be attached to pin X2A42 of the phyCARD Connector.

If the dedicated touch screen controller at U28 is chosen, the touch screen data is available at the I^2C interface of the X-Arc bus. The controller's slave address can be selected with jumper J3 (refer to *section 17.2.4*). The default address of the controller is 0x88 (write) and 0x89 (read). The interrupt output of the touch screen controller is connected to GPIO2 (GPIO2_IRQ, pin X2A47) which extends to port PE5 of the i.MX27 on the phyCARD-S.

17.3.8 Camera Interface (X5)

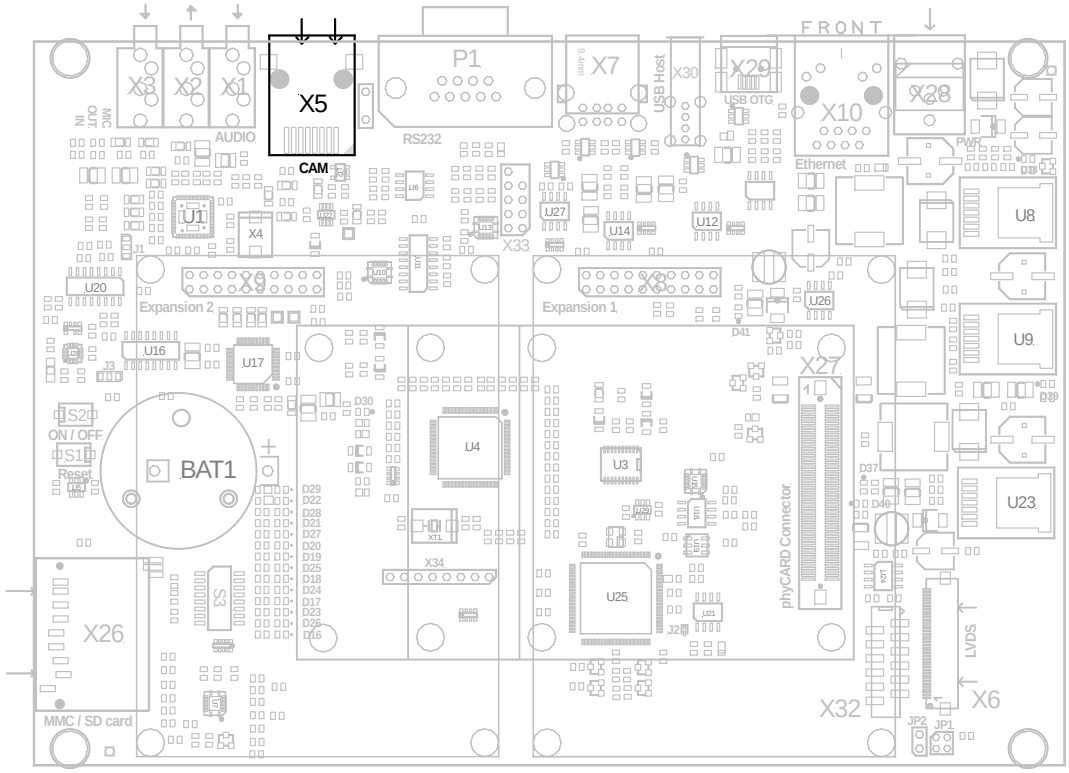

Figure 27: Camera interface at connectors X5

The phyCARD-S has an optional camera interface. This interface extends from the phyCARD-Connector to the RJ45 socket (X5) on the Carrier Board. The table below shows the Pin-out of connector X5:

Pin #	Signal Name	Description
1	RXIN+	LVDS Input+
2	RXIN-	LVDS Input-
3	RX_CLK-	LVDS Clock-
4	I2C_SDA	I2C Data
5	I2C_SCL	I2C Clock
6	RXCLK+	LVDS Clock+
7	VCC_CAM	Power supply camera (3.3V)
8	GND	Ground

Table 39: PHYTEC camera connector X5

17.3.9 Audio Interface (X1,X2,X3)

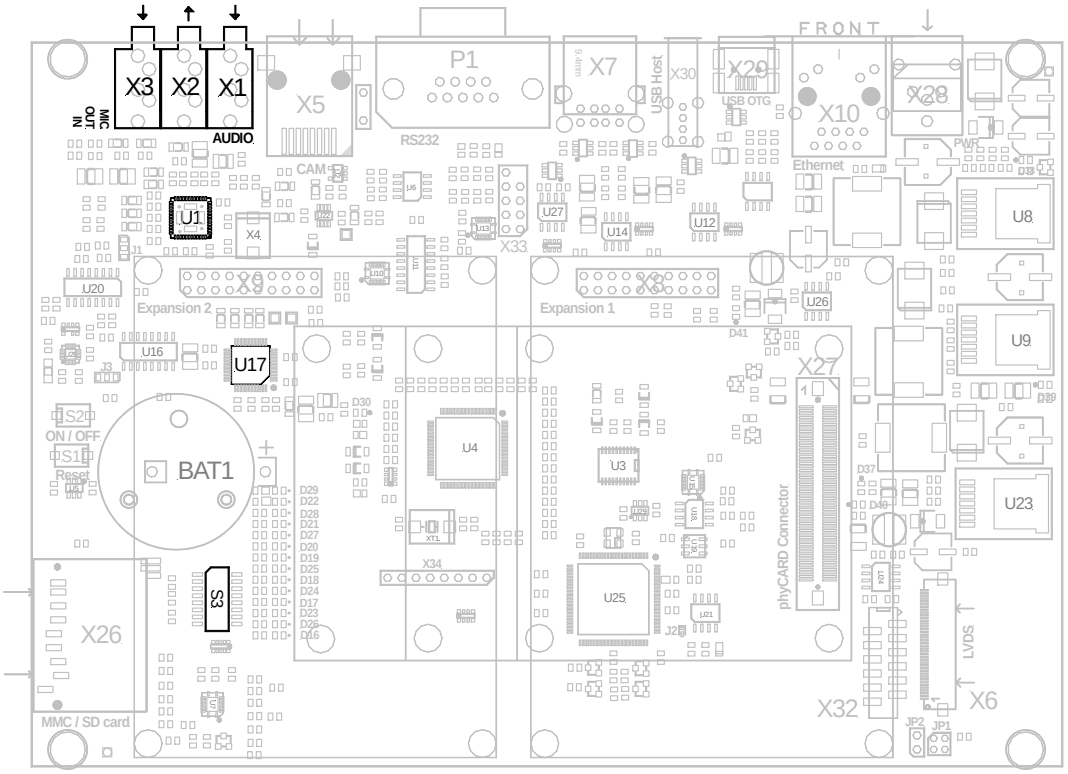

Figure 28: Audio interface at connectors X1,X2,X3

The AC97/HDA interface on the phyCARD connects to a Wolfson WM9712L (U1) or AD1986A (U17) audio codec controller on the Carrier Board. Switches 1 and 2 of DIP-Switch S3 select which codec is used to process the audio signals. *Table 40* shows the different options.

Button	Setting	Description
S3_1/ S3_2	**0/0**	**Wolfson audio/touch contrl. (U1) selected for touch and audio**
	0/1	Wolfson audio/touch contrl. (U1) selected for audio, dedicated touch contrl. (U28) for touch
	1/0	Analog Devices audio contrl. (U17) selected for audio, dedicated touch contrl. (U28) for touch

Table 40: Selection of the audio codec

Audio devices can be connected to 3,5mm audio jacks at X1, X2, and X3.

Audio Outputs:
X2 – Line Output - Line_OUTL/Line_OUTR

Audio Inputs:
X1- Microphone Inputs - MIC1/MIC2
X3 - Line Input - Line_INL/Line_INR

Please refer to the audio codec's reference manual for additional information regarding the special interface specification.

17.3.10 I²C Connectivity

The I²C interface of the X-Arc bus is available at different connectors on the phyBASE. The following table provides a list of the connectors and pins with I²C connectivity.

Connector	Location
Camera interface X5	pin 4 (I²C_SDA); pin 5 (I²C_SCL)
Display data connector X6	pin 8 (I²C_SDA); pin 7 (I²C_SCL)
Expansion connector 1 X8A	pin 7 (I²C_SDA); pin 8 (I²C_SCL)
Expansion connector 2 X9A	pin 7 (I²C_SDA); pin 8 (I²C_SCL)

Table 41: I²C connectivity

To avoid any conflicts when connecting external I²C devices to the phyBASE the addresses of the on-board I²C devices must be considered. Some of the addresses can be configured by jumper. *Table 42* lists the addresses already in use. The table shows only the default address. Please refer to *section 17.2.4* for alternative address settings.

Device	Address used (write / read)	Jumper
LED dimmer (U21)	0xC0 / 0xC1	J2
RTC (U3)	0xA2 / 0xA3	
A/D converter (U22)	0xC8 / 0xC9	
Touch screen controller (U28)	0x88 / 0x89	J3
CPLD (U25)	0x80 / 0x81	S3_3, S3_4

Table 42: I^2C addresses in use

17.3.11 SPI Connectivity

The SPI interface of the X-Arc bus is available at the expansion connectors X8A and X9A as well as at the display data connector X6 (refer to *sections 17.3.7.1* and *17.3.13* to see the Pin-out). Due to the X-Arc bus specification only two slave select signals are available. Because of that the CPLD maps the SPI interface to two of the connectors depending on the configuration of switches 7 and 8 of DIP-Switch S3. The table below shows the possible configurations.

Button	Setting	Description
S3_7/ S3_8	**0/0**	**SS0/GPIO0[11] -> expansion 0 (X8A), SS1/GPIO1[1] -> expansion 1 (X9A)**
	0/1	SS0/GPIO0[1] -> expansion 0 (X8A), SS1/GPIO1[1] -> display data connector (X6)
	1/x	SS0/GPIO0[1] -> expansion 1 (X9A), SS1/GPIO1[1] -> display data connector (X6)

Table 43: SPI connector selection

[11] : GPIO0 ≙ PC31 and GPIO1 ≙ PC25 of the i.MX27

17.3.12 User programmable GPIOs

Two (GPIO0_IRQ and GPIO1_IRQ) of the three GPIO / Interrupt signals available at the X-Arc bus are freely available. They are mapped to the expansion connectors X8A and X9A (pin 16), or to the display data connector X6 (pin 5) depending in the configuration at DIP-Switch S3 (see *Table 43*). The third GPIO I Interrupt signal (GPIO2_IRQ) is used to connect the interrupt output of the touch screen controller at U28 to the phyCARD-S.

17.3.13 Expansion connectors (X8A, X9A)

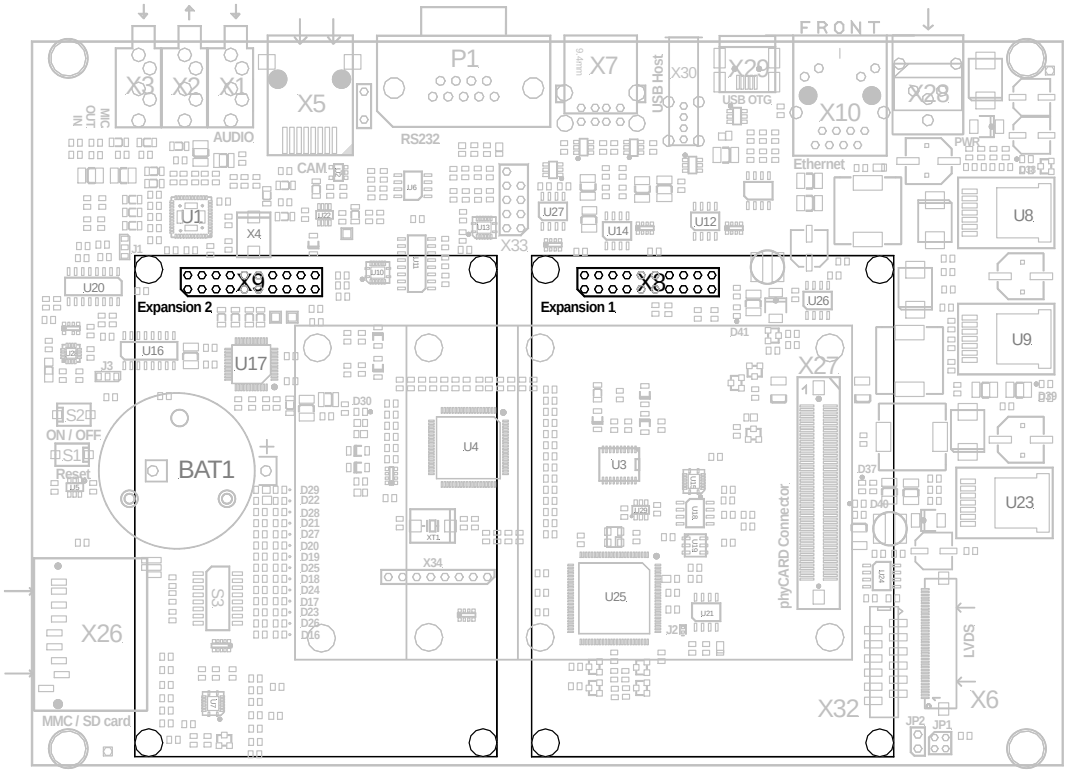

Figure 29*: Expansion connector X8A, X9A*

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The expansion connectors X8A and X9A provide an easy way to add other functions and features to the phyBASE. Standard interfaces such as USB, SPI and I^2C as well as different supply voltages and one GPIO are available at the pin header rows.

As can be seen in *Figure 29* the location of the connectors allows to expand the functionality without expanding the physical dimensions. Mounting wholes can be used to screw the additional PCBs to the phyBASE.

The expansion connectors share the SPI interface and the GPIOs of the X-Arc bus with the display data connector X6. Therefore switches 7 and 8 of DIP-Switch S3 must be configured to map the signals to the desired connector.

Button	Setting	Description
S3_7/ S3_8	**0/0**	**SS0/GPIO0[12] -> expansion 0 (X8A), SS1/GPIO1[1] -> expansion 1 (X9A)**
	0/1	SS0/GPIO0[1] -> expansion 0 (X8A), SS1/GPIO1[1] -> display data connector (X6)
	1/x	SS0/GPIO0[1] -> expansion 1 (X9A), SS1/GPIO1[1] -> display data connector (X6)

Table 44: SPI and GPIO connector selection

Pin #	Signal Name	Description
1	VCC5V	5V power supply
2	VCC5V	5V power supply
3	VCC3V3	3,3V power supply
4	VCC3V3	3,3V power supply
5	GND	Ground
6	GND	Ground
7	I2C_SDA	I^2C Data
8	I2C_SCL	I^2C Clock

[12] : GPIO0 ≙ PC31 and GPIO1 ≙ PC25 of the i.MX27

9	GND	Ground
10	GND	Ground
11	SPI_SS_SLOT0 SPI_SS_SLOT1	X8A SPI chip select expansion port 0 X9A SPI chip select expansion port 1
12	SPI1_MOSI	SPI master output/slave input
13	SPI1_SCLK	SPI clock output
14	SPI1_MISO	SPI master input/slave output
15	/SPI1_RDY	SPI data ready input master mode only
16	SLOT0_IRQ SLOT1_IRQ	X8A Interrupt input expansion port 0 X9A Interrupt input expansion port 1
17	GND	Ground
18	GND	Ground
19	USB3_D- USB4_D-	X8A USB3 Data D- X9A USB4 Data D-
20	USB3_D+ USB4_D+	X8A USB3 Data D+ X9A USB4 Data D+

Table 45: PHYTEC expansion connector X8A, X9A

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17.3.14 Security Digital Card/ MultiMedia Card (X26)

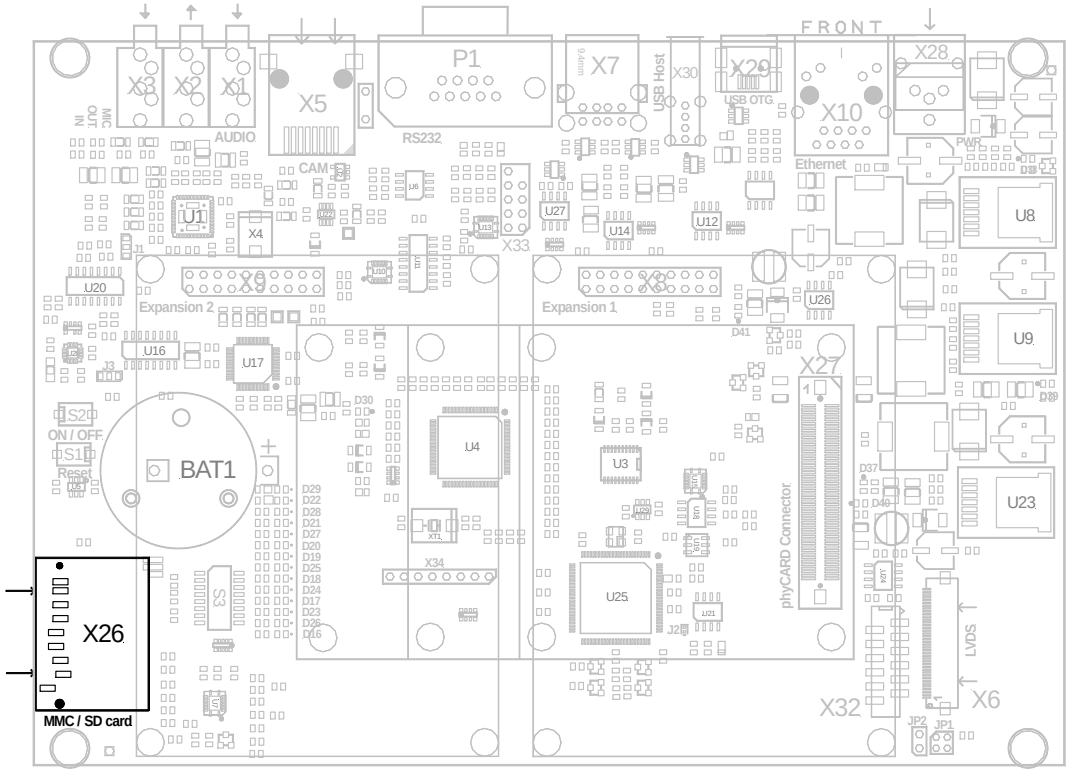


Figure 30*: SD Card interface at connector X26*

The phyCARD Carrier Board provides a standard SDHC card slot at X26 for connection to SD/MMC interface cards. It allows easy and convenient connection to peripheral devices like SD- and MMC cards. Power to the SD interface is supplied by sticking the appropriate card into the SD/MMC slot. The card slot X26 connects to the phyCARD-S via a level shifter to ensure the correct voltage for the SD/MMC cards.

17.3.15 Boot Mode Selection (JP1)

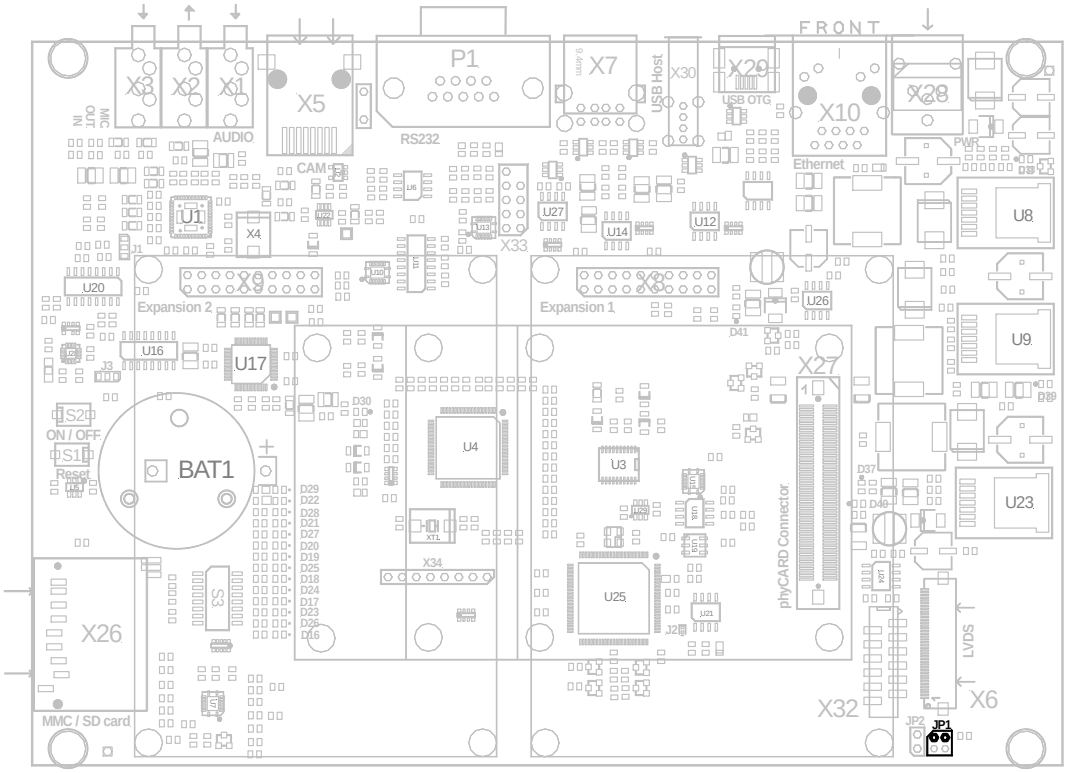


Figure 31*: Boot Mode Selcetion Jumper JP1*

The boot mode jumper JP1 is provided to configure the boot mode of the phyCARD-S after a reset.

By default the boot mode jumper is open, configuring the phyCARD-S for booting from the Flash device. Closing jumper JP1 results in start of the on-chip boot strap software of the i.MX27. Please refer to the phyCARD-S Quick Start Manual as well as the i.MX27 Reference Manual for Information on how to use the boot strap mode.

Jumper	Setting	Description
JP1	**open**	Jumper JP1 selects the boot device of the phyCARD-S **FLASH enabled as Boot device**
	1+2	internal ROM of the i.MX27 enabled as Boot device and thus starting the bootstrap program
		other settings must not be used with the phyCARD-S

17.3.16 System Reset Button (S1)

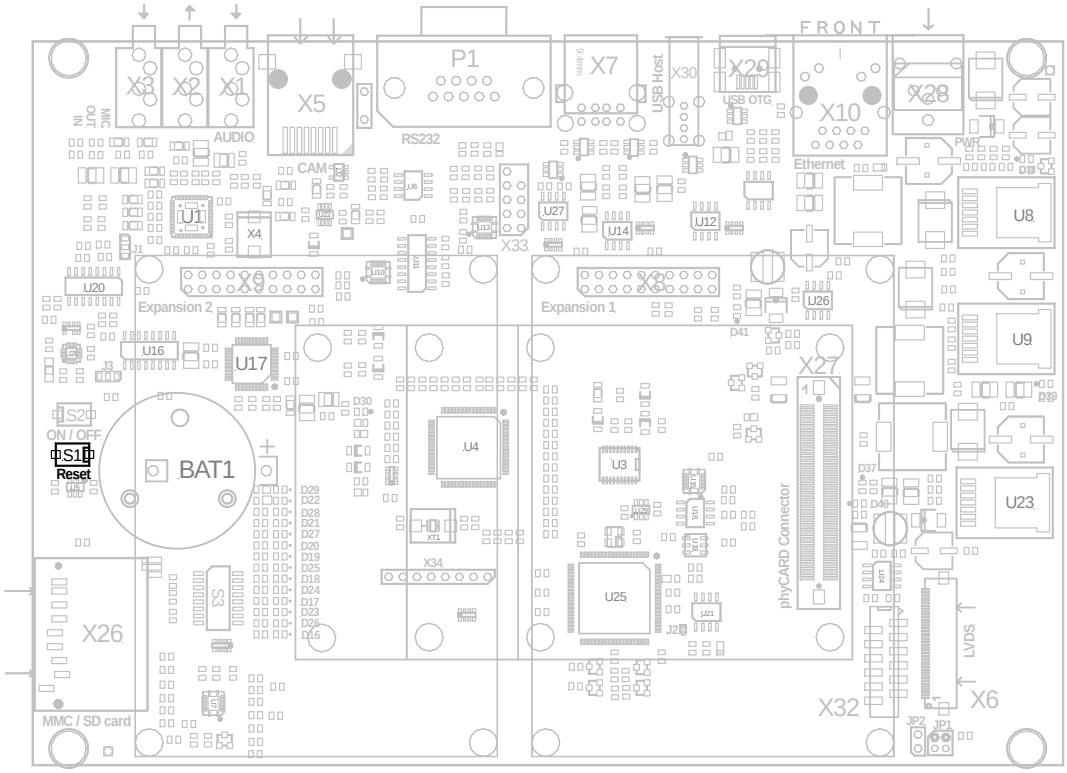
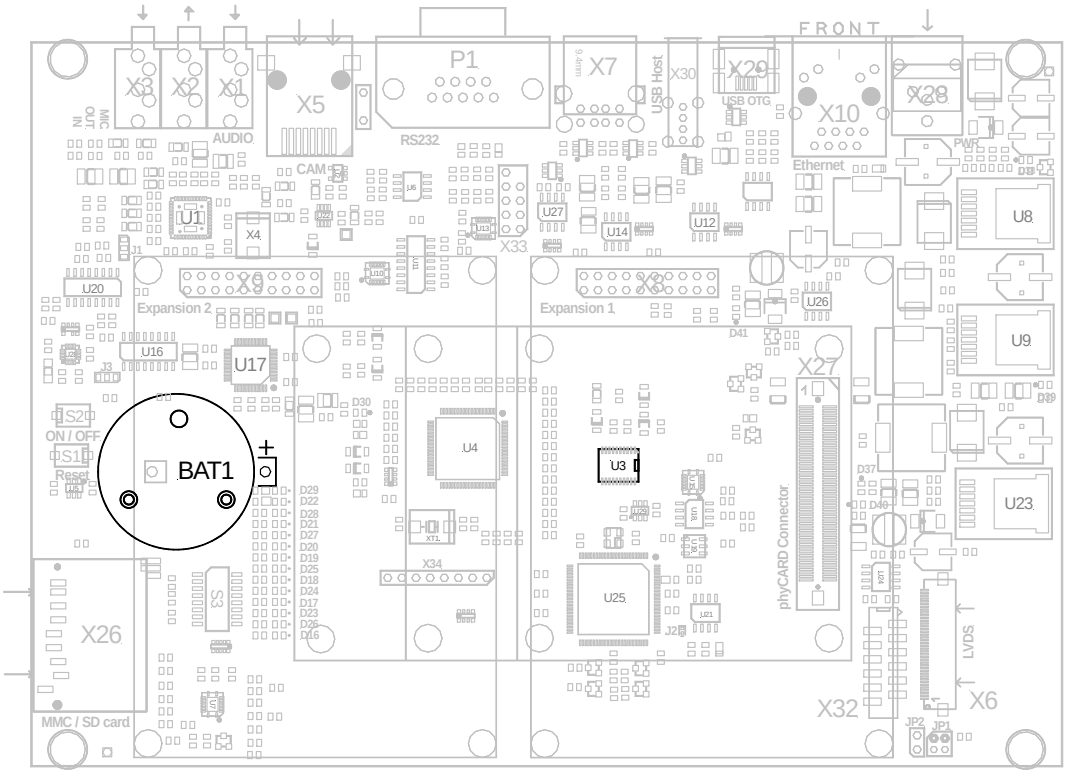


Figure 32*: System Reset Button S1*

The phyCARD Carrier Board is equipped with a system reset button at S1. Pressing the button will not only reset the phyCARD mounted on the phyBASE, but also the peripheral devices, such as the USB Hub, etc.

17.3.17 RTC at U3



For real-time or time-driven applications, the phyBASE is equipped with an RTC-8564 Real-Time Clock at U3. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0xA2(write)/0xA3(read)
- Power consumption
  Bus active (400 kHz): < 1 mA
  Bus inactive, CLKOUT inactive: = 275 nA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

The Real-Time Clock is programmed via the I^2C bus (address 0xA2 / 0xA3). Since the phyCORE-S is equipped with an internal I^2C controller, the I^2C protocol is processed very effectively without extensive processor action (refer also to *section 9.5)*

The Real-Time Clock also provides an interrupt output that extends to the Wakeup signal at X27A48. An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications.

If the RTC interrupt is to be used as a software interrupt via a corresponding interrupt input of the processor.

Note:
After connection of the supply voltage the Real-Time Clock generates no **interrupt. The RTC must be first initialized (see *RTC Data Sheet* for more information).**

Use of a coin cell at BAT1 allows to buffer the RTC.

17.3.18 PLD at U25

The phyBASE is equipped with a Lattice LC4256V PLD at U25. This PLD device provides the following features:

- Power management function (*section 17.3.2*)
- Signal mapping for sound devices WM9712L and AD1986A (*section 17.3.9*)
- Configuration the sound device AD1986A for HDA or AC97
- Signal mapping SPI chipselect and interrupt to the expansion or display connectors (*sections 17.3.11* and *17.3.12*)
- Touch Signal mapping to WM9712L or STMP811 (*section 17.3.7.3*)

17.3.19 Carrier Board Physical Dimensions

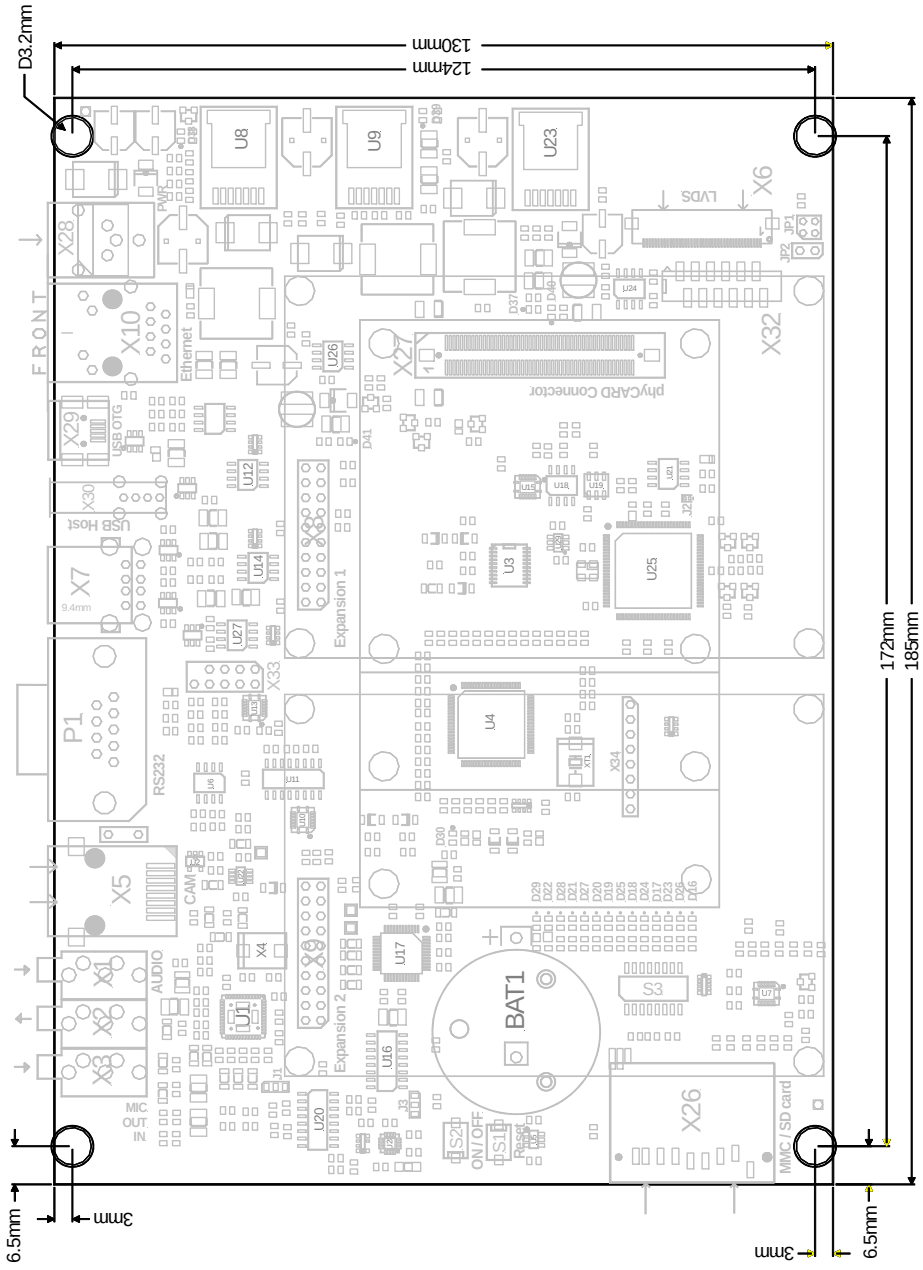


Figure 33: Carrier Board Physical Dimensions

Please contact us if a more detailed dimensioned drawing is needed to integrate the phyBASE into a customer application.

18 Revision History

Date	Version numbers	Changes in this manual
01-07-2009	Manual L-731e_0	First draft, Preliminary documentation. Describes the phyCARD-S with phyBASE- Baseboard.
05-05-2010	Manual L-731e_1	

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Document: phyCARD-S
Document number: L-731e_1, April 2010

How would you improve this manual?

Did you find any mistakes in this manual? page

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Ordering No. L-731e_1
Printed in Germany